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Via-Hole Filling with Molybdenum by RF Bias Sputtering

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RF bias sputtering has been found to be effective for planarized via-hole filling under the high resputtering condition. Planarized via-hole filling without sputter-induced defects in a Si substrate was accomplished by two step substrate bias change deposition. By using the two step RF bias sputtering, the via-hole was completely filled. The step height on the Mo film surface on the via-hole was reduced to half the initial via-hole depth. Furthermore, the film surface slope over the via-hole step became very gentle (~15°). These features are favorable for multi-level interconnection formation in VLSIs.

1. Introduction

For realizing reliable fine-line multi-level interconnection and three-dimensional ICs, surface planarization is indispensable not only for interlevel insulation layers but also for metal layers.

RF bias sputtering has been widely studied due to its unique feature wherein both film deposition and planarization take place in a vacuum chamber simultaneously/continuously. Although RF bias sputtering has been usually applied to planarized insulator deposition[1,2], it was also applied to planarized aluminum film deposition recently[3]. However, filling via-holes with a metal film to form a planarized surface (planarized via-hole filling) is also very important to fabricate planarized multi-level interconnection.

This paper reports planarized via-hole filling with molybdenum (Mo) by RF bias sputtering. Mo was chosen due to its refractory nature and its high electromigration resistance.

2. Experiment

A planar magnetron RF bias sputtering system was used to fill the via-holes, as shown in Fig.1. Sample substrates were placed on a 2mm thick SiO_2 plate which covered the stainless steel substrate holder. Two RF generators were used in this system in order to indepedently control the power supplied to the target and the power supplied to the substrate holder. The vacuum chamber was pumped down to 1 X 10^{-4} Pa pressure before introducing argon gas. Mo films were deposited with 1kW target power (5.5W/cm^2 target power density) and 0.4 Pa argon pressure. Sample structure was CVD SiO_2 with via-holes on a Si substrate. The via-hole side walls were nearly perpendicular to the substrate surface. Substrate DC bias voltage (Vsub) is the negative DC voltage induced by the RF substrate bias between the substrate holder and ground potential. Vsub was used as a parameter. No substrate heating/cooling was employed. After the Mo film deposition, samples were cleaved nearly at the center of the via-holes with deposited Mo and observed by SEM.

3. Results and Discussion

3.1. Effective deposition rate

Figure 2 shows the relation between the Mo effective deposition rates (Deff) on horizontal substrate surface and Vsub, with target power as a parameter. Deff decreases linearly with increasing |Vsub|. This means that sputter-etching (resputtering) effect on substrate surface increases with |Vsub| increase. Deff decrease-rates are nearly the same for 0.5kW and 1kW target power values. Because Deff is equal to the difference between the deposition rate and etching rate, the same decrease-rates indicate that the etching rate does not depend on the target power, but depends on the substrate bias.

3.2. Substrate bias voltage effects

The deposited Mo film topographies in via-holes depend on Vsub, as shown in Fig.3. The via-hole was 2.5µm in diameter and 1.2µm in depth. All Mo films were deposited to an about 1.2µm thickness on horizontal SiO_2 surface, which is equal to the via-hole depth.

When Vsub values were 0V or -200V, Mo films deposited on via-hole side walls became coarse, probably due to the shadowing effect caused by the overhang grown from the via-hole step shoulder. For Vsub over -400V, the deposited Mo film on the via-hole side walls became dense and the taper angle (θ_1) for deposited Mo film surface on via-hole step decreased, as shown in Fig.4. When the Vsub value was over -500V, as shown in Fig.3(c), the deposited Mo film in the via-hole bottom (d_1) became thicker than that on the horizontal SiO_2 surface outside the via-hole (d_2). When the Vsub value was at -600V, as shown in Fig.3(d), the via-hole was completely filled with Mo film. In addition, the taper angle for the Mo film on the via-hole step shoulder was reduced to 15°. However, defects were induced along the via-hole bottom edge in the Si substrate. Further increase in the Vsub value to -700V caused severe surface roughening in the deposited Mo films. These results revealed that the Mo film deposition on via-holes by RF bias sputtering accomplished planarized via-hole filling. The Vsub value suitable for planarized via-hole filling was -500V ~ -600V.

3.3. Via-hole filling process

A series of SEM micrographs, as shown in Fig.5, reveal how the via-holes were filled with Mo as sputtering time elapsed. The Mo depositions were performed with 1kW target power and with -600V Vsub at different sputtering time. As mentioned previously, this condition has a planarization effect, characterized by the via-hole step height reduction due to the larger d_1 than d_2 and the taper angle moderation for the film deposited on the via-hole step shoulder.

In 5 minutes, the deposited Mo film on the via-hole side walls was dense and film hardly deposited on the via-hole step shoulder due to resputtering. In 5 and 15 minutes, d_1 was nearly equal to d_2. The taper angle of deposited film on the via-hole step shoulder was 30°. The deposited film on the via-hole side walls was thicker than that on the bottom. After 20 minutes film deposition, the d_1 value became larger than the d_2 value. The d_1 to d_2 ratio was about 1.5 and the taper angle on the via-hole step shoulder was decreased to 20°. In 33 minutes, thickness ratio did not change, but the taper angle was further reduced to 15°.

In order to clarify the film deposition mechanism, the amount of Mo deposited in a via-hole (Vin), including the Mo deposited on via-hole side walls, and the amount of Mo deposited on the same area as the via-hole on horizontal surface outside the via-hole (Vout) was plotted as a function of deposition time, as shown in Fig.6. Vin and Vout were calculated by using the cross sectional Mo film topographies. The Vin increase rate (Rin) was twice as much as the Vout increase rate (Rout), up to about 15 ~ 20 minutes deposition time. However, after 20 minutes, Rin decreased to nearly the same level as Rout.

This results and the Mo film topography time dependence are explained as follows. In the early stage of the via-hole filling (up to 5 minutes), since Ar ions incidented perpendicular to the substrate, the via-hole side walls were steep and the solid angle subtended by the top circle of the via-hole at any place inside the via-hole was small, the amount of Mo resputtered from the via-hole side walls would be small and the probability for Mo resputtered from the via-hole bottom surface to redeposit on the side walls would be high. Therefore, Vin was larger than Vout by nearly the amount of Mo deposited on the via-hole side walls. As more sputtering time elapsed, the deposited Mo film on the via-hole side walls formed a ~60° slope and the horizontal area inside the via-hole was smaller than the initial via-hole bottom area, as shown in Fig.5 (b). That is, unfilled part in the via-hole formed an inverse cone. The Mo resputtering rate on the lower angle side walls in this stage is expected to become gradually higher than that before this stage and roughly the same as that for the horizontal area. Furthermore, the solid angle at the via-hole interior became larger. Thus, Rin would be gradually reduced. In the latter half time (from 20 minutes to 33 minutes), Rin was decreased to the same level as Rout. Because the unfilled part in the via-hole formed an inverse cone, d_1 became larger than d_2 . Because of perpendicular incident Ar ions to the substrate, the Mo resputtered from the side walls at this stage (15 ~ 20 min.) is considered to be ejected mainly in the via-hole bottom direction and redeposit around the via-hole bottom. This effect would also contribute to the larger d1 than d2.

3.4. Planarized via-hole filling

The planarized via-hole filling without sputter-induced defects in a Si substrate was accomplished by two step substrate bias change. The first step was thin film deposition at a lower substrate bias to protect the Si surface from resputtering. The second step was planarized filling at a higher bias. Figure 7 shows a cross sectional SEM micrograph of the Mo film deposited on a 2.5μm diameter, 1.2μm deep via-hole. The Mo film was deposited with target power at 1kW. The first step was carried out at -400V for 3 minutes and the second step was carried out at -600V for 40 minutes. The deposited Mo film completely filled the via-hole. The film surface step height was reduced to half the original via-hole step height. The surface step angle was reduced to ~15°. Defects along the via-hole bottom edge were not induced in this technique.

4.Conclusion

Filling via-holes with Mo using RF bias sputtering has been studied.

It was found that, under an appropriate substrate bias range, the shadowing effect at the via-hole step disappeared. Mo was completely filled into the via-hole. Also, the step height was reduced to half the original step height, owing to redeposition for the resputted Mo in the via-hole. The step angle, orginally ~90° , was greatly reduced to ~15° . From observations on via-hole cross sections for different sputtering times, redeposition on the via-hole side walls was found to play a major role in the step height reduction. Planarized via-hole filling with Mo without resputter-induced defects was achieved by changing the substrate bias in two steps. The two step RF bias sputtering technique, characterized by simultaneously interconnect metal layer deposition and planarized via-hole filling, is expected to be useful in VLSI and three dimentional IC fabrication.

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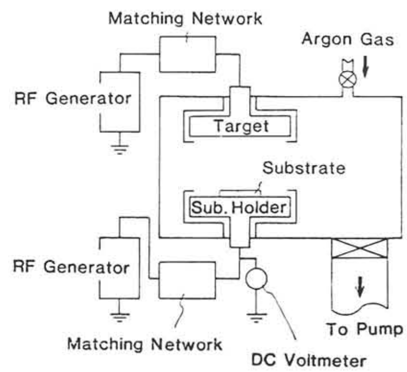


Fig.1 RF bias sputtering system.

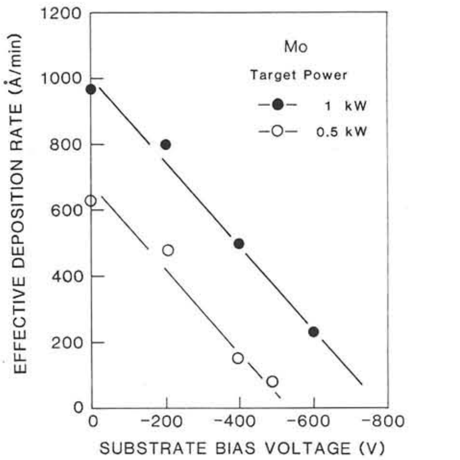


Fig.2 Mo effective deposition rate vs. substrate bias voltage.

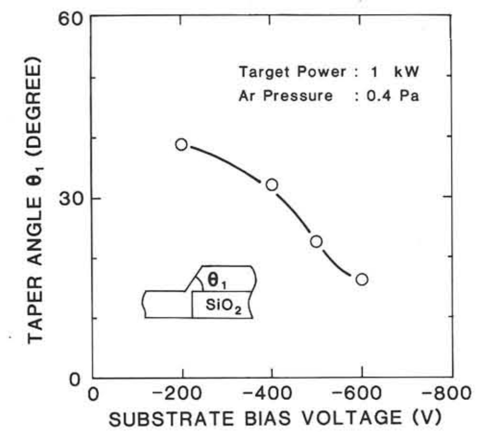


Fig.4 Taper angle for deposited Mo film vs. substrate bias voltage.

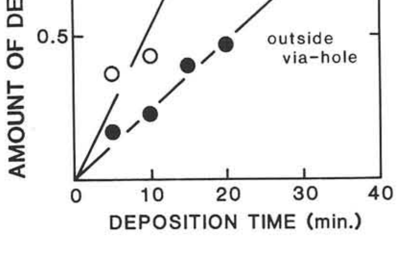
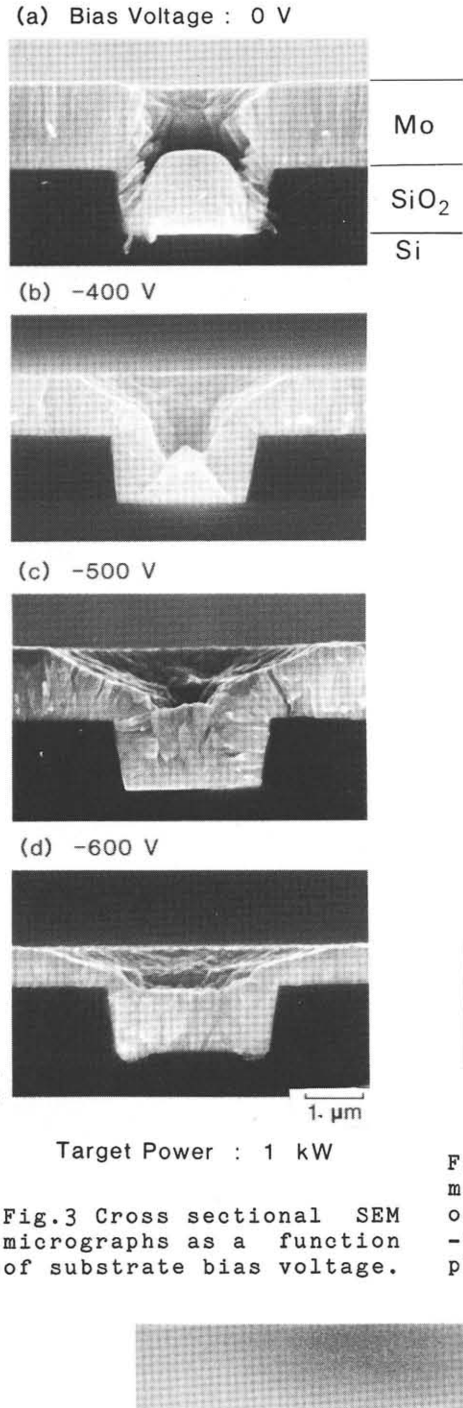
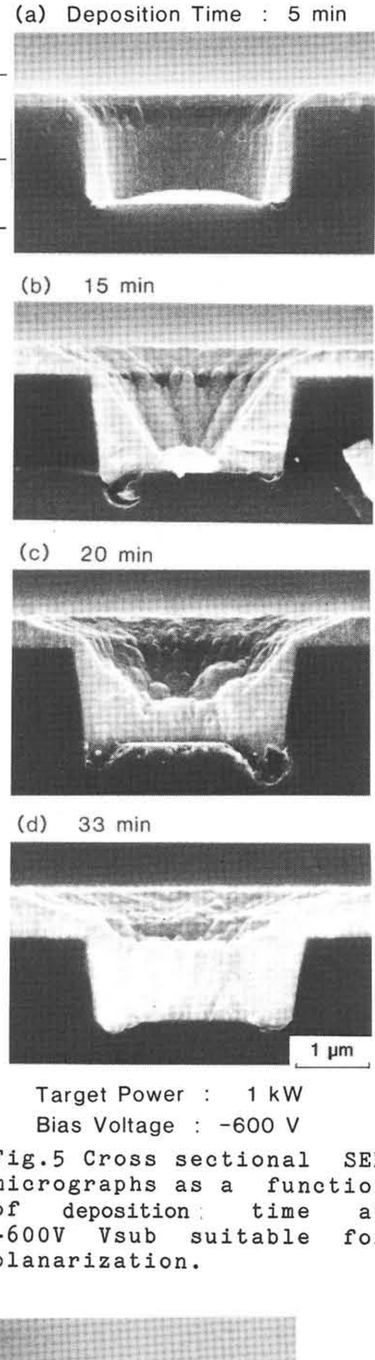


Fig.6 Amount of deposited Mo vs. deposition time.



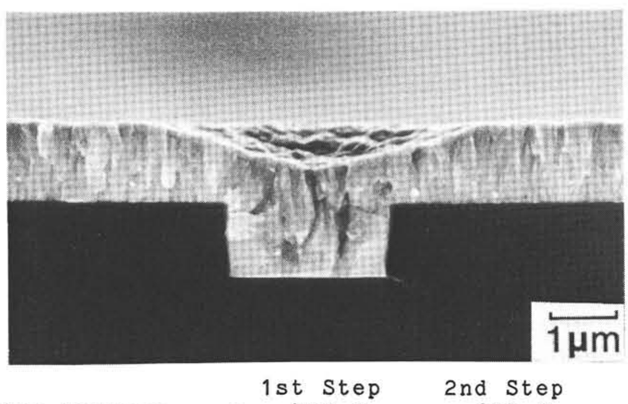
Target Power : 1 kW

Fig.3 Cross sectional SEM micrographs as a function of substrate bias voltage.



Target Power : 1 kW
Bias Voltage : -600 V

Fig.5 Cross sectional SEM micrographs as a function of deposition time at -600V Vsub suitable for planarization.



		1st Step	2nd Step
Bias voltage	:	-400 V	-600 V
Deposition rate	:	3 min	40 min

Fig.7 Cross sectional SEM micrograph after planarized via-hole filling by two step substrate bias change.