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Possibilities and Limitations of Bipolar Devices

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ABSTRACT

The problems faced by the conventional bipolar technology are reviewed and the potential as well as limitations of the advanced "double-poly" self-aligned bipolar technologies are discussed. Also discussed are the technology concerns in scaling these advanced bipolar transistors for both high-performance ECL and low-power VLSI circuits.

I. INTRODUCTION

The very rapid progress in MOS technology in recent years has extended MOS into applications, such as gate array[1] and static RAM[2] traditionally provided by bipolar. However, at the same time, bipolar technology has also made such rapid progress that it not only maintains its leadership in the very high-performance applications[3,4] but has also demonstrated its VLSI potential[5]. In this paper, we review the problems faced by the conventional bipolar technology in scaling and put into perspective the potential as well as the limitations of the advanced bipolar devices.

II. INTRINSIC DEVICE AND CIRCUIT CHARACTERISTICS

The exponential I-V relationship gives bipolar devices much higher transconductance and hence much better "threshold voltage" control than MOS devices. As a consequence of the excellent threshold voltage control, bipolar circuits can be designed with supply voltages V_S close to the minimum determined by the number of diode-drops in the circuit. Commonly used V_S values are 2.2 - 4.0V for ECL, 1.5 - 2.0V for ISL and STL, and 1.5 - 5.0V for TTL. V_S can be less than 1.0V for I^2L/MTL.

Another important consequence of the tight threshold voltage control is the very small logic swing V_L practical in bipolar circuits. V_L is typically 400 - 800 mV for ECL, 500 - 700 mV for I^2L/MTL, and merely 150 - 200 mV for ISL and STL. The high transconductance and small logic swing combine to give bipolar transistors the best capacitance - driving capability of all silicon devices.

The power-delay product can be expressed in the form $KC V_L V_S$, where K is a duty factor, C is the average loading capacitance including the device parasitic capacitance. For bipolar (static) circuits, K is between 0.5 and 1. NMOS dynamic circuits and CMOS circuits have the advantage of K being less than unity. However, the small V_L and V_S are definitely advantages of bipolar.

III. PROBLEMS WITH SCALING CONVENTIONAL BIPOLAR

Figure 1 illustrates the typical delay-power characteristics of a properly designed bipolar circuit. At low power, the delay is governed by the capacitance loading (including device parasitic capacitances). The minimum delay at high power dissipation is determined by the intrinsic base width.

Figure 2 shows the schematics of a typical state-of-the-art conventional bipolar transistor structure and an advanced "double-poly" self-aligned bipolar transistor structure[6]. The conventional bipolar device in general has such large parasitic capacitance that circuits must dissipate rather large power in order to have speeds approaching that limited by the base-width component.

To reduce the minimum delay in scaling, the vertical doping profile must be reduced. Unfortunately, when the emitter junction depth of a conventional bipolar transistor is thinner than about 300 nm, current gain degradation due to the shallow-emitter effect occurs[7]. In an effort to restore the current gain, designers often reduce the intrinsic base doping concentration, resulting in significantly reduced emitter-collector punch-through voltage[8]. Such incompatible design requirements imply that the conventional bipolar transistor cannot achieve much performance improvement in scaling beyond about 2 μm.

IV. ADVANCED BIPOLAR TECHNOLOGIES

Tremendous progress has been made in bipolar technology within the past few years. The three key advanced technology elements are (i) polysilicon base contact[6,9,10], (ii) trench isolation[6,11], and (iii) polysilicon emitter contact[4,6,7,9]. Both the polysilicon base contact, particularly the self-aligned version, and the trench isolation significantly reduce the device area and the associated parasitic capacitance, and hence significantly reduce the power-delay product and increase the density of bipolar circuits. The schematics in Fig. 2 illustrate the device area and capacitance reduction.

The ultimate ideal structure having minimum parasitic capacitance is achieved in the symmetrical transistors[3,10] illustrated in Fig. 3. Such symmetrical transistors have comparable upward and downward I-V characteristics which, when cleverly applied, can significantly improve circuit densities[3].

The polysilicon emitter contact provides a solution to the problem of insufficient current gain in scaled bipolar transistors[7] . Thus, the advanced "double-poly" bipolar transistors are not only fast and dense, but are also scalable to sub-micron dimensions.

V. SCALING PROPERTIES AND CONCERNS

(a) Scaling

It is clear from the device design optimization procedure[12] that there is no universal design. In other words, a design optimized for high-performance ECL is not necessarily optimal for low-power VLSI circuits such as I^2L/MTL and STL. The design procedure and the scaling rules for ECL have been described by Tang and Solomon[12,13].

From the process technology point of view, it is much more challenging to develop technologies for scaled ECL, due to its very shallow vertical doping profiles and very high current densities, than for VLSI circuits where the vertical doping profiles need not be very shallow and the current densities are much lower. This fundamental difference between high-performance and VLSI circuits should be kept in mind as we discuss the scaled device characteristics and technology concerns below.

(b) Device characteristics

As the base width is reduced in scaling, the base doping concentration must be increased to prevent punch-through[12,13]. Just as heavy-doping effect in the emitter increases the base current and decrease the current gain, heavy-doping effect in the base will increase the collector current and hence increase the current gain. For submicron ECL with base doping concentration greater than 10^{18} cm^{-3}, the effect of heavy doping can be quite significant[14] For wider-base VLSI circuits, this effect is minimal.

As the base doping is increased in scaling, the emitter-base junction tunneling current increases very rapidly. However, this tunneling current will remain negligibly small even for 0.5 μm ECL[15].

(c) Circuit Characteristics

Figure 4 shows the expected scaled self-aligned ECL circuit characteristics from Ref. 13. The power-delay characteristics should be even better for the symmetrical or SICOS transistor technology[3,10]. The problems, due primarily to the very high current density, that must be solved are formidable in order to achieve 0.25 μm ECL[13] . The 0.5 μm 50 ps ECL, on the other hand, is expected to be a challenging but achievable goal in the near future.

The potential of bipolar VLSI circuits remain pretty much an uncharted territory. The very limited work in this area[3,5,6] suggests that bipolar VLSI is surprisingly competitive with MOS in density and performance. As will be discussed later, bipolar VLSI circuits are much more readily scalable down to and perhaps beyond 0.5 μm than ECL. Based on the measured power-delay of 600 fJ for a FO=1 I^2L/MTL gate at 3 μm[3], one can project a power-delay potentially as low as 13 fJ for an I^2L/MTL gate with FO=3 in 0.25 μm SICOS technology.

(d) Schottky Barrier Diodes

Many bipolar circuits employ SBD's. It was shown recently[16] that the minority-carrier storage in SBD at high current densities is much less than previously predicted, indicating that SBD can be scaled without worrying about minority-carrier effect. However, it is likely that the series resistance will limit the miniaturization of SBD's in scaling.

(e) Concerns

Three of the often mentioned technology concerns in scaling bipolar devices are (i) pipe defects, (ii) electromigration, and (iii) contact resistance. In the absence of reported data relevant to the advanced bipolar technologies, we can only discuss these concerns qualitatively here.

Pipe defects are the result of localized enhanced diffusion of dopant impurities. In conventional bipolar processes where the deep emitter and base junctions are formed by diffusion drive-in, the very long thermal cycles help the formation of pipe defects. The use of ion implantation and polysilicon in advanced bipolar processes has greatly reduced the thermal cycles in the emitter and base formation, and hence should significantly reduce the probability of pipe defect formation.

The current density is expected to reach 5 x 10^5 A/cm^2 for 0.25 μm ECL[13]. Electromigration is definitely of great concern at such high current densities. For VLSI circuits operating at about 10 times lower current, electromigration effects should be minimal with advanced metallurgy. Furthermore, wider metal lines on upper interconnection levels can be used for power distribution to reduce electromigration concerns.

Contact resistance, particularly the emitter polysilicon/silicon contact resistance, is a concern in scaled bipolar transistors. Polysilicon emitter contact resistivity of about 7 x 10^{-7} Ω-cm^2 has been reported[16]. This value can fluctuate widely as the details of the emitter and base formation processes change, but will probably remain larger than 1 x 10^{-7} Ω-cm^2. For high-performance ECL, it may be necessary to purposely increase the emitter area to achieve an acceptable emitter contact resistance. For VLSI circuits operating at much lower currents, contact resistance, unless abnormally large, is probably of little concern.

VI. SUMMARY

The advanced "double-poly" self-aligned transistors are expected to be scalable down to at least 0.5 μm for high-performance ECL and to 0.25 μm and beyond for low-power VLSI circuits. Significant reduction in pipe defect density is expected from the reduced thermal cycles in these advanced technologies. 50 ps 0.5 μm ECL and 13 fJ 0.25 μm I^2L/MTL appear to be two of the many realizable potentials of scaled bipolar.

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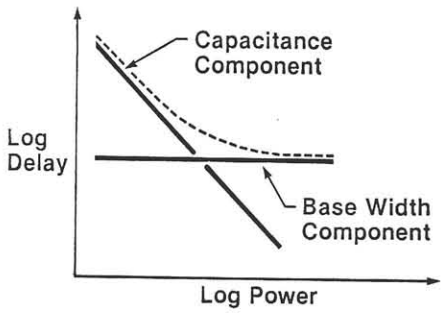

Fig. 1. Typical delay-power characteristics of a properly designed bipolar transistor.

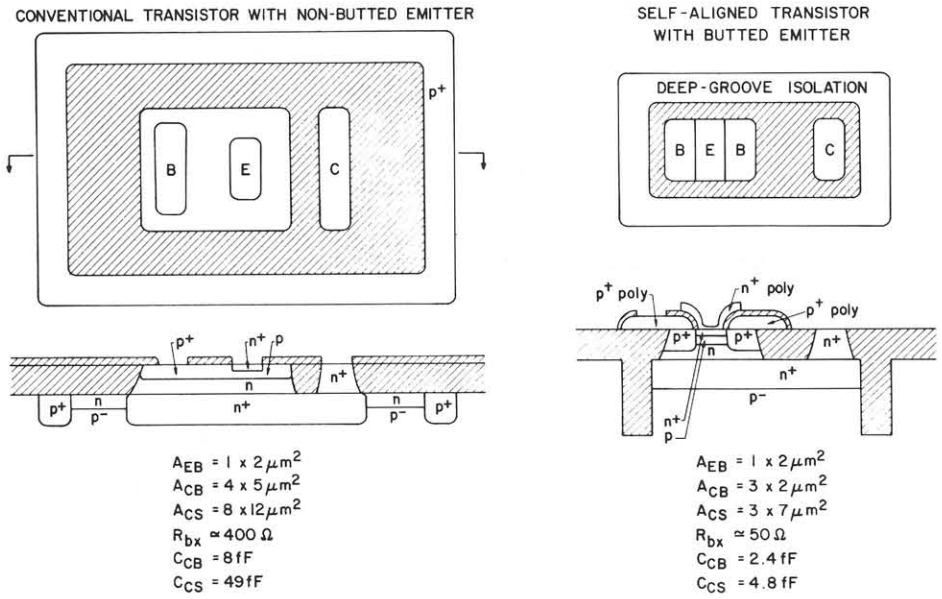

Fig. 2. Schematics of (a) a typical state-or-the-art conventional bipolar transistor structure, and (b) an advanced "double-poly" self-aligned bipolar transistor structure.

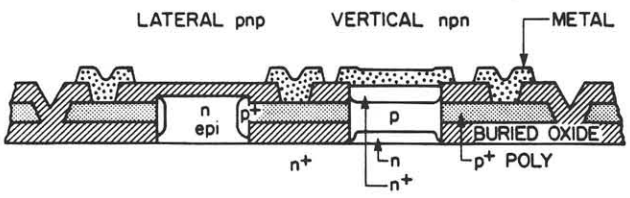

Fig. 3. Schematic of the ideal symetrical bipolar transistor structure (from Ref. 10).

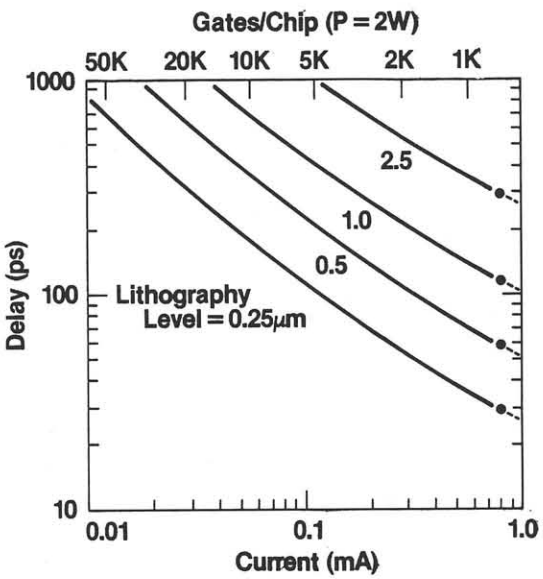

Fig. 4. Projected performance in scaling of an average loaded ECL circuit.