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# A 30 ps Si Bipolar IC Using Super Self-Aligned Process Technology

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New 30 psec Si bipolar IC technology has been developed by scaling down the lateral geometry and forming shallow junctions. An NPN transistor with a 0.35 μm-wide emitter and a 1.57 μm-wide base region is made using Super Self-aligned process Technology ( SST ). The $f_T$ values for this device are 13.7 GHz at a collector-emitter voltage of 1 V and 17.1 GHz at 3 V. Propagation delay times ( fanin = fanout = 1 ) of 30 psec/gate for non-threshold logic and 50 psec/gate for low-level current mode logic have been achieved.

## 1. INTRODUCTION

In order to achieve higher switching speeds, bipolar devices are being made with smaller lateral and vertical dimensions. One way to scale down the lateral dimension is to make use of the new 0.5 μm electron beam ( EB ) lithography. For example, a double-base NPN transistor can be reduced to 4 μm-wide in the base region if the masking tolerances for mis-alignment and side-etching are less than 0.25 μm ( Fig. 1-a ).

However, mis-alignment between the $N^+$ emitter and $P^+$ external base adversely affects such device characteristics as current gain ($h_{FE}$) and emitter-base junction breakdown voltage ($V_{EBO}$). The problem becomes more serious as the device is made smaller to switch at higher speed.

To solve this problem, a self-aligned bipolar process called Super Self-aligned process Technology ( SST [1],[2] ) has been developed. Using this process, only one photolithographical mask is needed to fabricate all of the active transistor regions, excluding tolerance areas for mis-alignment ( Fig.1-b ). The lateral dimension of a device can be greatly reduced without lowering of, or producing variation in, current gain and breakdown voltage. Miniaturized structures with an emitter window 0.35 μm wide and base region 1.57 μm wide have been realized, as shown in Fig. 2. The base region is less than half that of a device fabricated using 0.5 μm EB lithography. This lateral down-scaling reduces base resistance and junction capacitance.

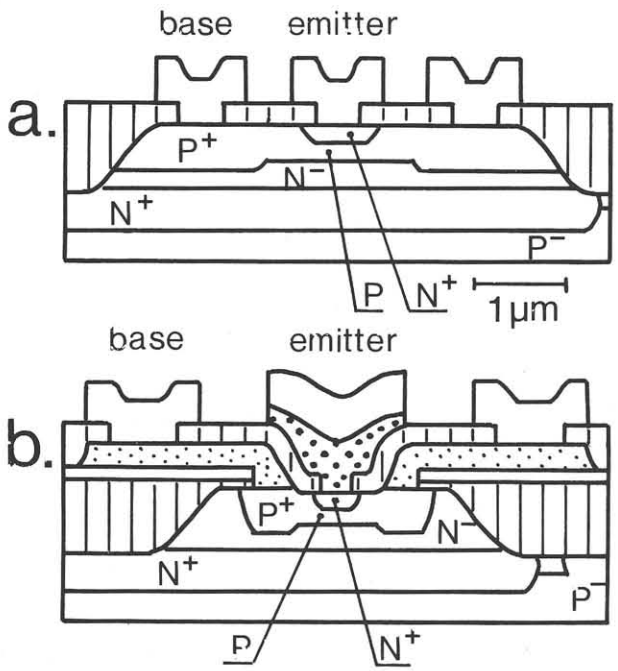


Fig. 1. Cross-sectional views of a 0.5 μm planar transistor ( 1-a ) and an SST transistor ( 1-b ).

In addition, heavily doped polysilicons are used for emitter and base electrodes and diffusion sources, thus making it possible to form stable shallow junctions. At the same time, this vertical down-scaling achieves a shorter transit time ( $T_F$ ) and a higher cut-off frequency ( $f_T$ ).

By reducing the base resistance, junction

capacitances and transit time, transistors are made to switch at very high speed, such as 30 psec/gate for non-threshold logic ( NTL ) and 50 psec/gate for low-level current mode logic (LCML).

## 2. DEVICE STRUCTURE

A cross-sectional view of SST, represented by a scanning electron microphotograph, is shown in Fig. 2. Emitter width, spacing between emitter and base contacts, and base contact width are 0.35 μm, 0.26 μm and 0.35 μm, respectively. Thus, this scaling down in the lateral dimension leads to significant lowering of the base resistance and junction capacitances.

Emitter-base spacing is uniformly fabricated with high accuracy because no mask alignment is necessary. Therefore, uniform current gain and breakdown voltage are obtainable.

Heavily doped $N^+$ and $P^+$ polysilicons are used for the emitter and base electrodes and diffusion sources. This makes it possible to form stable shallow junctions of about 100 nm. This vertical scaling down produces shorter transit time and a higher cut-off frequency.

Furthermore, the base layer is formed by double boron ion implantation ( I/I ). The first ion implantation forms an intrinsic base. The second ion implantation, with an impurity concentration peak at the silicon surface, adds P-type impurity to the boundary between the Si and $SiO_2$ in the external base region. This process reduces external base resistance and surface recombination current under the $SiO_2$ between the emitter and base. This low recombination results in higher current gain in the low collector current ( $I_C$ ) range.

Consequently, high speed switching is achieved by down-scaling in the lateral and vertical dimensions.

## 3. FABRICATION PROCESS

The fabrication steps for SST, as shown schematically in Fig. 3, are:

(1) The $SiO_2$, $Si_3N_4$ and polysilicon are formed sequentially. Then the polysilicon over the transistor active regions, such as the emitter and base, is etched away. This area is determined by photolithographical patterning with

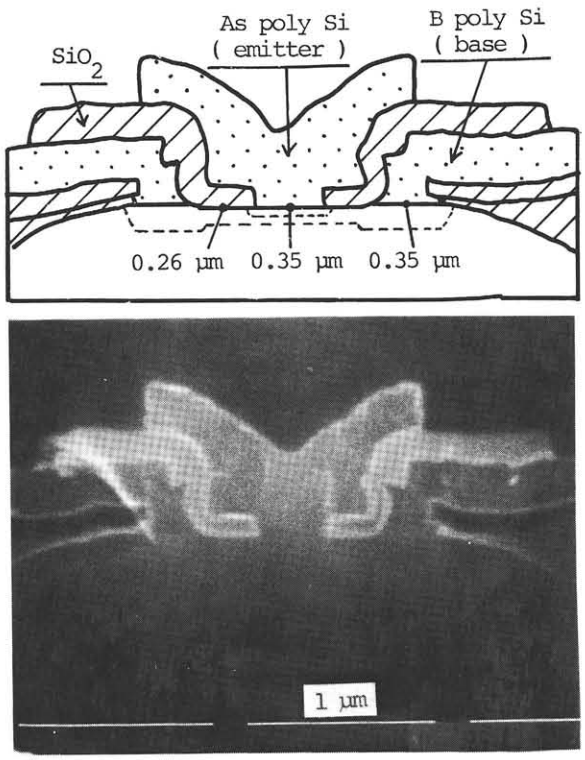


Fig. 2. Cross-sectional view of an SST with a 0.35 μm emitter as observed by SEM.

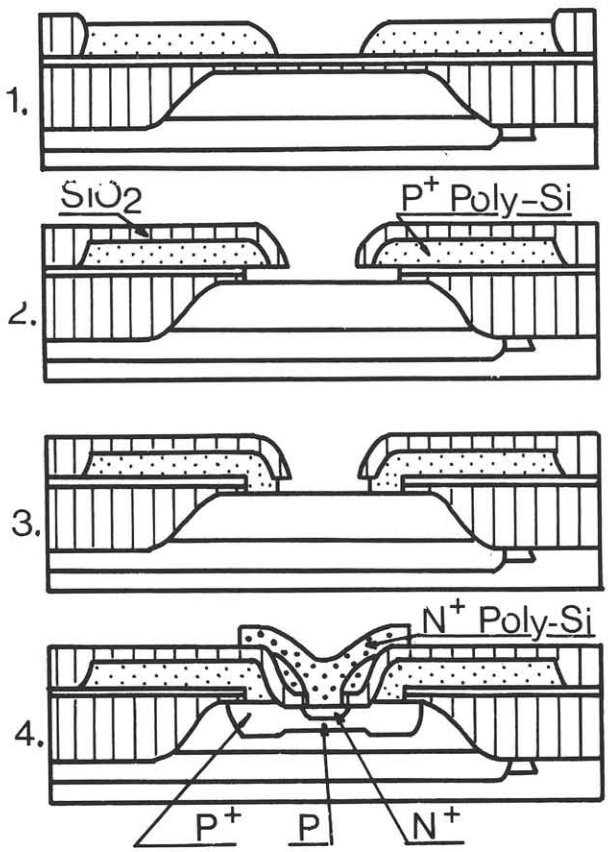


Fig. 3. SST fabrication steps.

only one mask.

(2) The $P^+$ polysilicon is oxidized. Then the $Si_3N_4$ under the base polysilicon is side-etched and the $SiO_2$ is removed.

(3) The second polysilicon layer is deposited isotropically to fill the space under the base polysilicon. Then this polysilicon, except where it is view for base contact, is removed. The base polysilicon electrodes come into contact with the silicon substrate.

(4) The $SiO_2$ over both the silicon substrate and the polysilicon side-wall is formed thermally. Double boron ion implantation form the intrinsic base. $SiO_2$ and polysilicon are deposited, and are anisotropically etched by reactive ion etchings. Then the emitter window is opened. The emitter is formed by arsenic diffusion from heavily ion implanted polysilicon. The first Al-Si wiring of the 1.5 μm line and 1 μm spacing is formed.

Thus all the active regions are formed using only one mask.

## 4. EXPERIMENTAL RESULTS

Current gain vs. collector current characteristics for two types of SST with emitters 16 μm long are shown in Fig. 4. One has a 0.35 μm-wide emitter and a base formed by double ion implantation. The other has a 0.5 μm-wide emitter and a base formed by single implantation. The double ion implanted device has sufficient current gain over the 1 nA to about 1 mA current range. This transistor has higher current gain in the low collector current range than the single implantation transistor, resulting from its lower recombination current. Furthermore, the SST with the 0.35 μm emitter maintains a current gain as high as that with a 0.5 μm emitter in the high current range, in spite of the extremely narrow emitter.

Cut-off frequency vs. collector current ($V_{CE}$) characteristics were obtained by measuring the S parameters over the 200 MHz to 3 GHz frequency range, as shown in Fig. 5. The test transistor has 10 emitter stripes with areas of 0.35 x 16 $\mu m^2$. The maximum $f_T$ values were 13.7 GHz at $V_{CE}$ of 1 V and 17.1 GHz at $V_{CE}$ of 3 V. The maximum values were obtained at a current density of about 30 KA/$cm^2$. The transit time is obtained

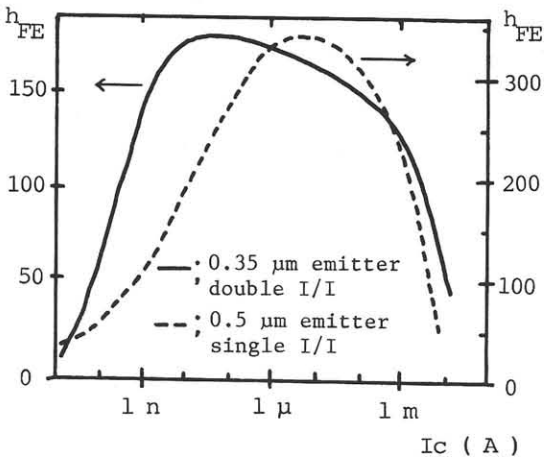


Fig. 4. Current gain ( $h_{FE}$ ) vs. collector current ( $I_C$ ) characteristics for two types of SST with 16 μm long emitters. One has a 0.35 μm-wide emitter and a base formed by double ion implantation ( I/I ). The other has a 0.5 μm-wide emitter and a base formed by single implantation.

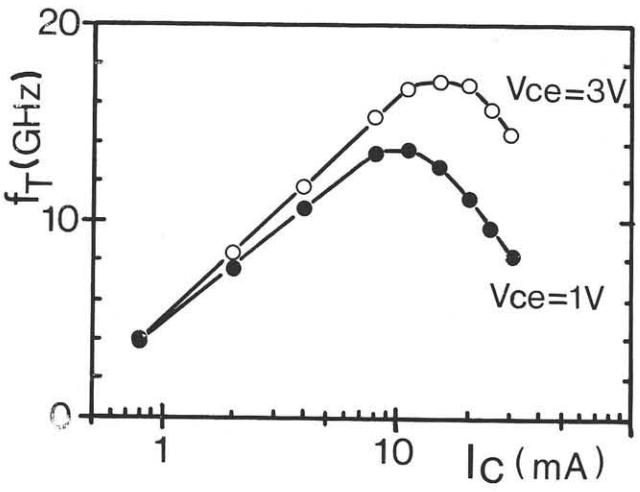


Fig. 5. Cut-off frequency ( $f_T$ ) vs. collector current ( Ic ) characteristics for an emitter with a 0.35 x 16 $\mu m^2$ x 10 area at collector-emitter voltages ( $V_{CE}$ ) of 1 V and 3 V.

| | | |
|---|---|---|
| $T_F$ | 8.4 | ps |
| $R_B$ | 310 | ohm |
| $R_E$ | 18.5 | ohm |
| $R_C$ | 62.4 | ohm |
| $C_{CB}$ | 7.4 | fF |
| $C_{EB}$ | 10.4 | fF |
| $C_{CS}$ | 22.9 | fF |
| $V_{EBO}$ | 5.7 | V |
| $V_{ECO}$ | 6.1 | V |

Table 1. Characteristics of an SST with a 0.35 x 5 $\mu m^2$ emitter.

from the $f_T$-$I_C$ curve. Transit time was 8.4 psec at 1 V and 7.0 psec at 3 V.

The characteristics of the SST with 0.35 x 5 $\mu m^2$ emitter are summarized in Table 1, including capacitances and resistances. As shown, the collector capacitance and base resistance were reduced to 7.4 fF and 310 ohms, respectively. The emitter-base breakdown voltage was as high as 5.7 V.

## 5. PERFORMANCE

High speed switching characteristics of the SST were evaluated using two different 51-stage ring oscillators ( fanin = fanout = 1 ): one with non-threshold logic ( NTL ) and the other with low-level current mode logic ( LCML ). The propagation delay times ( $t_{pd}$ ) are shown in Fig. 6 for devices having 5 μm and 10 μm long emitters with 0.35 μm-width, related to power dissipation. For the NTL, using transistors with a 0.35 x 10 $\mu m^2$ emitter, 30 psec/gate was achieved at 1.48 mW/gate. For the LCML, using 0.35 x 5 $\mu m^2$ emitters, 50 psec/gate was achieved at 1.46 mW/gate. The fastest output waveform for an NTL with 400 mV logic swings is shown in Fig. 7.

Arsenic doped polysilicon resistances and metal/insulator/metal capacitances are used in these ICs. The insulator is plasma-enhanced chemical vapor deposited silicon-nitride.

The delay times were also calculated using a circuit simulator ( SPICE ), based on the measured device parameters listed in Table 1. The calculated results were in good agreement with the experimental values, as shown in Fig. 6. These results indicate that high speed switching has been achieved by improving such device parameters as the junction capacitances, base resistance and transit time.

## 6. CONCLUSION

To achieve high speed switching, a bipolar transistor using SST was reduced in both the lateral and vertical dimensions without lowering current gain or breakdown voltage. The emitter window and base region were 0.35 μm and 1.57 μm wide, respectively. The $f_T$ values were 13.7 GHz ($V_{CE}$ = 1 V) and 17.1 GHz ($V_{CE}$ = 3 V). Propagation delay times of 30 psec/gate for NTL and 50 psec/gate for LCML have been achieved.

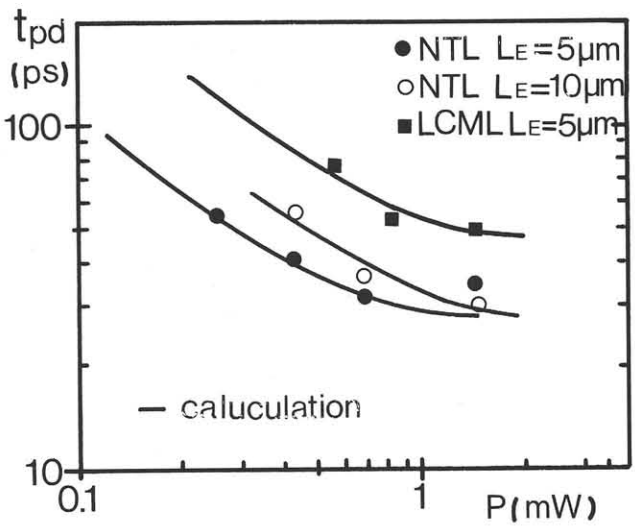


Fig. 6. Measured propagation delay times and power dissipation of NTL and LCML for emitter length ( $L_E$ ) of 5 μm and 10 μm, compared with simulated results using SPICE.

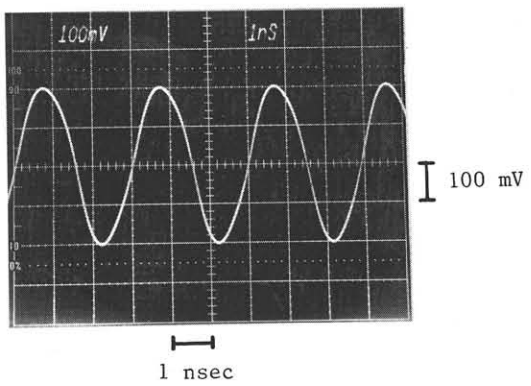


Fig. 7. Fastest output waveform for a 51-stage NTL ring oscillator with a 0.35 x 10 $\mu m^2$ emitter.


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