Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 213-216

A-4-3

Giga Hertz Band Tunable Limiting Amplifier Using Bipolar Super Self-Aligned Process Technology

Yukio Akazawa,* Katsushi Iwashita,** Noboru Ishihara,*
Shinsuke Konaka* and Mamoru Ohara*

* Atsugi Electrical Communication Laboratory, NTT, Atsugi-shi, Kanagawa 243-01, Japan

** Yokosuka Electrical Communication Laboratory, NTT, Yokosuka-shi, Kanagawa 238-03, Japan

An electrically controllable giga-hertz band tuning amplifier IC and limiting amplifier IC will be described. Bipolar Super Self-Aligned Process Technology (SST) which yields a sub-micron emitter stripe transistor with 17GHz-ft is applied. Tuning frequency is adjusted electrically using an external PIN diode chip to compensate for the on-chip element fluctuations. Cascade connection of these ICs achieves complete limiting operation at 1.8GHz with small phase-shift deviation under 10 degrees over the input dynamic range from -42 to -14dBm. The results demonstrate the feasibility of monolithic integration of a timing circuit in very-high-capacity optical systems.

§1. Introduction

Recently, requirements of high-capacity communication systems have been steadily increasing. This has produced a strong requirement for monilithic amplifier ICs to achieve highly reliable, power efficient, compact communication systems.

Tuning and limiting functions are very fundamental in various communication systems including optical transmission and satellite communication systems. A resonant circuit consisting of L and C are essential to realizing a tuning amplifier. However, in monolithic ICs these elements are difficult to integrate on the same chip because of large manufacturing fluctuations and space factors. Still more, external elements can not be utilized to the GHz band due to difficulty in fine adjustment.

The limiting amplifier operation requires that phase shift variation between input and output signals be small over a wide dynamic range of input signal level. Gallium Arsenide IC technology is one alternative for realizing amplifiers that can operate at ultra high frequencies with small phase shift. However, problems such as low yield or insufficiency of gm for 50 ohm low line impedance systems remain.

A useful alternative is an improved Si-bipolar technology, SST 1). It yields a self-aligned sub-micron emitter stripe transistors of 17GHz-ft. Using the SST-process and new circuit technology, tuning and limiting amplifier ICs have been developed.

This paper describes the design and measured performance of these ICs.

§2. Circuit design

2.1 Tuning amplifier

Tuning frequency of on-chip resonant circuits deviates from designed values owing to fluctuations in inductance and capacitance. Thus, if discrete devices are used, fine adjustment of tuning frequency is needed. However, adjustment is very difficult because of the very small time constant. Further, there is the problem of tuning frequency deviation by physical shock.

Therefore, this design incorporated an external PIN diode chip to adjust tuning frequency electrically. The resonant circuit inductor was formed in a spiral pattern on the same chip as the amplifier circuit.

The tuning amplifier circuit configuration is shown in Fig. 1. The first stage is the tuning stage with LC resonant circuit. The second is the gain stage and the third is the wide band output matching stage to the 50 ohm line.

Simulated tuning characteristics and gain dependency against resonant capacitance C of the first tuning stage are shown in Fig. 2. Parastic capacitances of the on-chip inductor were considered as shown in Fig. 2. The decrease in gain is due to Q decrease for the overall tuning circuit containing transistor parastic elements. If

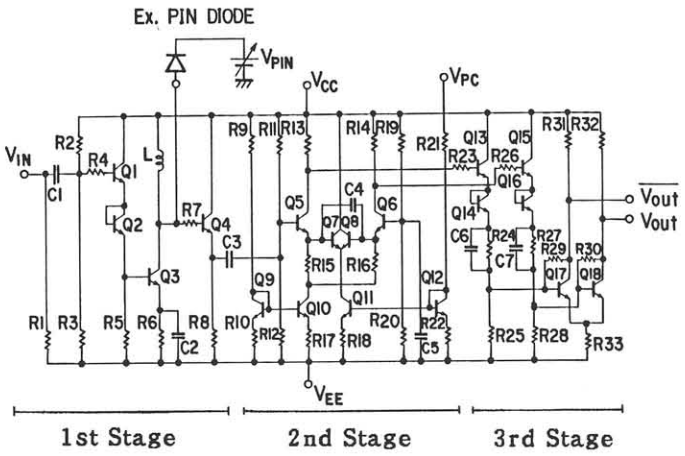

Fig. 1 Circuit configuration of the tuning amplifier.

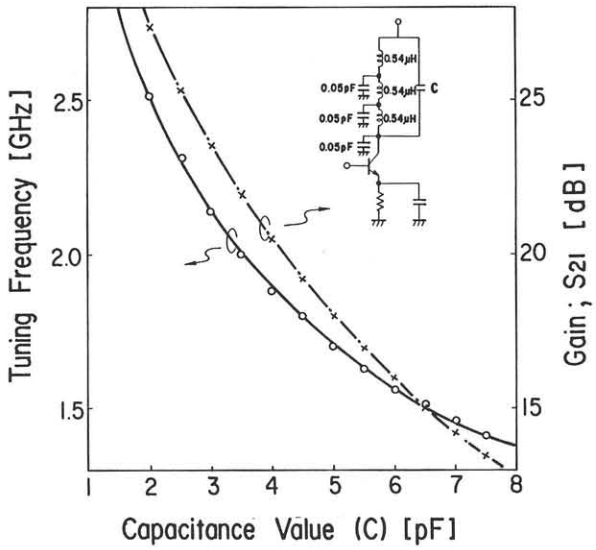

Fig. 2 Effect of resonant capacitance on the gain and the resonant frequency.

only the inductance value of L can be made larger, Q and gain will increase. However, since parastic resistance and capacitance of L increase at the same time, actual Q and gain can not be improved. Still more, the chip area becomes larger. Considering the above conditions and variable capacitance value of PIN diode, L of resonant circuit was designed as a 1.62nH rectangle spiral coil. The number of turns is 4 and line width is 10 μm. The second stage is a differential amplifier with a new adjustable peaking function to improve gain at high frequency. 2) The peaking circuit consists of Q7, Q8, Q11, Q12, R18, R21 and R22. By controlling terminal voltage Vpc, the base to emitter capacitances of Q7 and Q8 can be varied. This varies peaking capacitance of the amplifier so as to cause peaking in the high frequency region.

The third stage is a parallel feed back amplifier. Output impedance at low frequency is expressed by equation (1);

$$Rout = \frac{R29 + (R24 // R25 // RinQ)}{1 + \beta \cdot (R24 // R25 // RinQ)} // RoQ \quad (1)$$

, where *RinQ* is input impedance of Q27 or Q28, *RoQ* is output impedance of Q27 or Q28 and β is a common emitter circuit current gain of Q27 or Q28. Capacitors C6 and C7 were added to compensate for the output impedance increase in the high frequency region.

2.2 Limiting amplifier

A differential amplifier generally has many phase-shift mechanisms such as input voltage offset or unbalancing between differential outputs. 3) In this design, single-ended form was adopted for its small phase diviation.

Basic circuit configuration is shown in Fig. 3. The limiting characteristic is obtained as follows: When input voltage is low, Q1 is OFF and Q2 is ON. Therefore, output voltage is about 1 Vbe. At that time, Q5 saturates, though there is no degradation of the ac characteristic. On the other hand, when input valtage is high, Q1 is ON and Q2 is OFF. Current flowing in R2 is limited by Q5 and output voltage is restricted to $(Vcc - I \cdot R2 - Vbe)$, where I is the current value of the current source consisting of Q4, Q5 and R4.

Bias condition is very stable because Q1 is biased in the active region near cut off by R3 automatically. Voltage gain at low frequencies is expressed by equation (2), when diode resistance of Q5 is nealy equal to 0:

$$Gv = \frac{gm1}{(1 + gm1 \cdot Rsat)} \cdot \frac{R1 \cdot (gm2 \cdot R2 - 1)}{(1 + gm2 \cdot R1)} \quad (2)$$

, where *Rsat* is C-E saturation resistance of Q5 and *gm1* and *gm2* are transconductance of Q1 and Q2, respectively.

If $Rsat = 0$ and $gm2 \cdot R1 \gg 1$, $gm2 \cdot R2 \gg 1$, equation (2) is reduced to equation (3):

$$Gv = gm1 \cdot R2 \quad (3)$$

The dc transfer characteristics calculated by varying R1 as a parameter are shown in Fig. 4.

Fabricated circuit configuration of the limiting

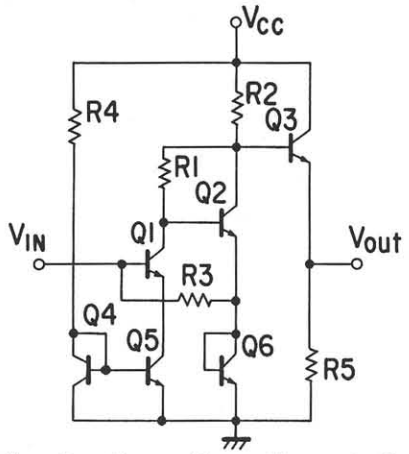

Fig. 3 Basic circuit configuration of the limiting amplifier.

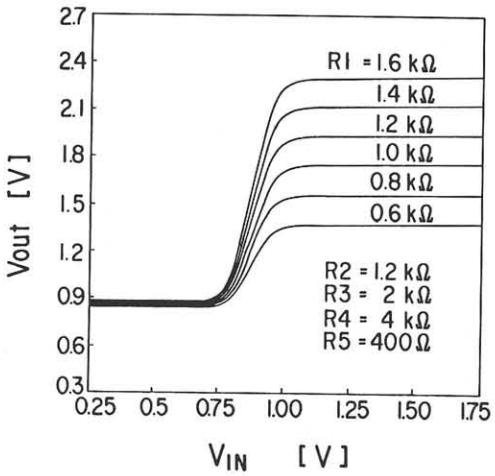

Fig. 4 DC transfer characteristics of the basic limiting amplifier.

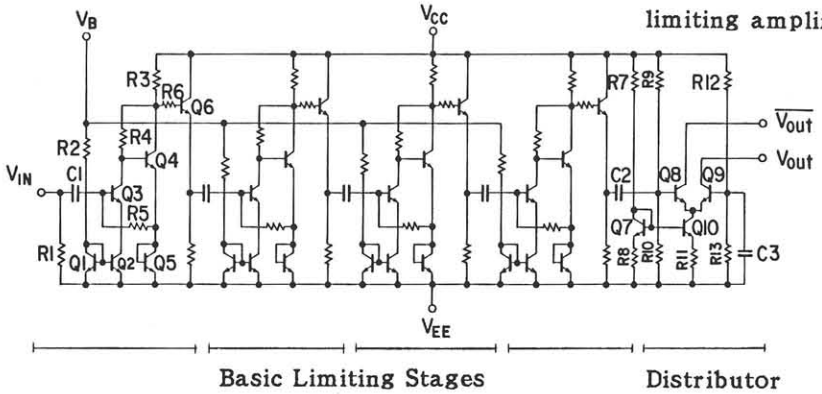

Fig. 5 Circuit configuration of the limiting amplifier.

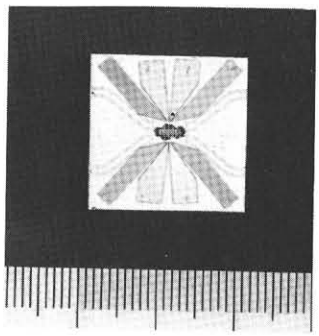

Fig. 8 Chip mounting ceramic plate.

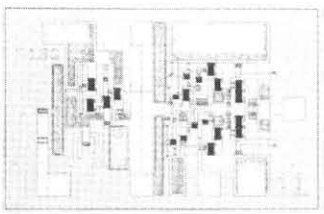

Fig. 6 Microphotograph of the tuning amplifier IC. (1mmx1.5mm)

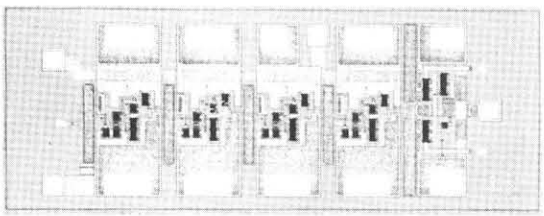

Fig. 7 Microphotograph of the limiting amplifier IC. (1mmx2.5mm)

amplifier which consists of 4 basic limiting stages and a distributor circuit is shown in Fig. 5. To achieve stable operation, the current source value was made to be adjustable by varying terminal voltage VB. This current value is sensitive to stability.

2.3 Chip layout

Chip photographs of the tuning and the limiting amplifier ICs are shown in Fig. 6 and Fig. 7. A common GND and dc feeding lines were separated by stage to prevent a coupling for forming through these lines.

§3. Measured performances

3.1 Chip mounting

A ceramic plate for evaluation, on which the IC chip is mounted, is shown in Fig. 8. Ample isolation of the input and output is neccessary for stable operation. For that purpose, lowering the impedance of dc supply line and reducing the coupling between input/output signal line are needed. Therefore, a grounded-co-planar line was used as the signal lines and a high-permitivity ceramic thin sheet of 500pF capacitance was used for dc feeding lines.

3.2 Performance

Frequency responses of S21, S11 and S22 as well as tuning frequency controllability of the tuning amplifier are shown in Fig. 9. Tuning frequency can be varied over the 1.4 ~ 1.85GHz range and 17dB gain was obtained at 1.8GHz.

Frequency responses of the limiting amplifier are shown in Fig. 10. Gain is 32dB at 1.8GHz.

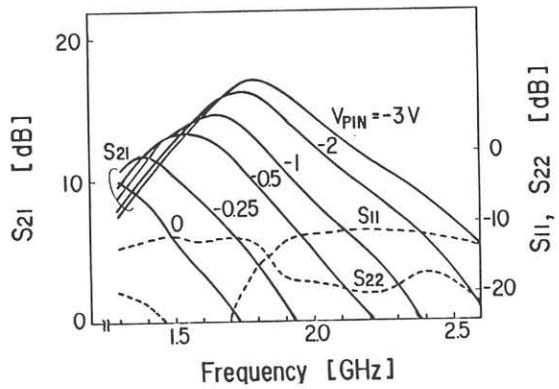

Fig. 9 Frequency responses of S21, S11 and S22 and tuning frequency controllability of the tuning amplifier.

Phase-shift and limiting charcteristics of the tunable limiting amplifier, measured at 1.8GHz using these ICs are shown in Fig. 11. Complete limiting operation with very small phase-shift deviation under 10 degrees is achieved over the input dynamic range from -42 to -14dBm. The output waveform is shown in Fig. 12.

Measured characteristics are summarized in Table-1.

§4. Conclusion

A wide dynamic range from -42 to -14dBm with very small phase-shift deviation under 10 degrees at 1.8GHz has been achieved by two ICs.

These ICs can be applied to very high capacity optical fiber transmission systems. 4)

Acknowledgements

The authors wish to express their thanks to Drs. H. Mukai, T. Sudo, A. Iwata, T. Sakai, Y. Aoyama, K. Kawarada and K. Nakagawa for their useful suggestions and comments. The authors also wish to thanks those who helped fabricate these ICs.

References

1) S. Konaka, Y. Yamamoto, and T. Sakai "A 30psec Si-Bipolar IC Using Super Self-Aligned Process Technology", on this conference.

2) M. Ohara, Y. Akazawa, N. Ishihara and S. Konaka ; IEEE J. Solid-State Circuit **SC-18** August (1984).

3) M. Aiki ; Paper Tech. Group, on CS, IECE Jpn. **CS81-132** (1981) (in Japanese).

4) K. Nakagawa, K. Iwashita, M. Ohara and S. Horiguchi ; ICC'84, proceedings **Vol. 2**, pp. 771-774, 1984.

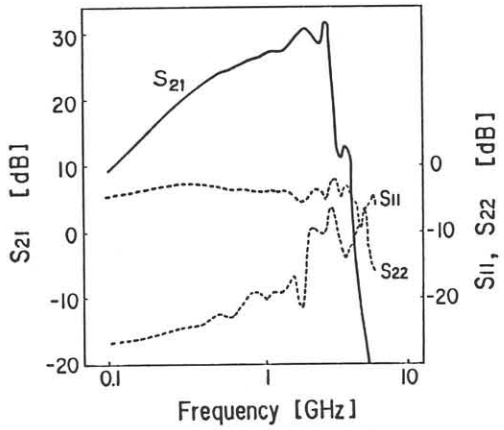

Fig. 10 Frequency response of the limiting amplifier.

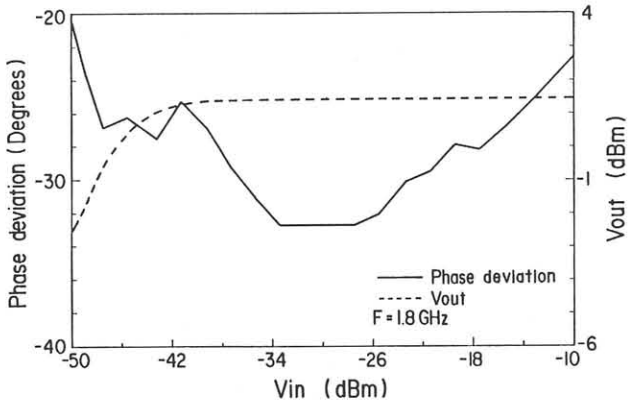

Fig. 11 Phase-shift and limiting characteristic of the tunable limiting amplifier.

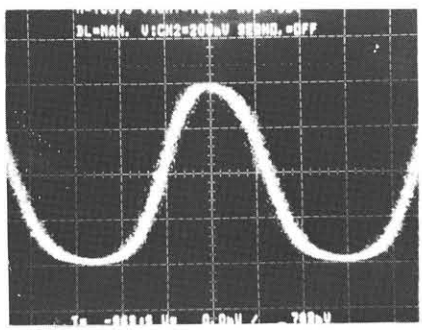

Fig. 12 Output wave form of the tunable limiting amplifier. (H:100pS/div, V:200mV/div)

Table 1 Measured Characteristics

	Tuning Amp.	Limiting Amp.	Tim.+Lim.	Unit
3dB band width	——	~2.7	——	GHz
Gain S_{21} *	17	32	52	dB
Input return loss *	−16	−14	−16	dB
Output return loss *	−14	——	——	dB
Input dynamic range **	——	——	−42~−14	dBm
Output signal level	——	0.8	0.8	V_{PP}
Power dissipation	700	260	960	mW
Chip size	1×1.5	1×2.5	——	mm^2

* at 1.8 GHz
** Phase deviation within 10 degree