Giga Hertz Band Tunable Limiting Amplifier
Using Bipolar Super Self-Aligned Process Technology

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An electrically controllable giga-hertz band tuning amplifier IC and limiting amplifier IC will be described. Bipolar Super Self-Aligned Process Technology (SST) which yields a sub-micron emitter stripe transistor with 17GHz-ft is applied. Tuning frequency is adjusted electrically using an external PIN diode chip to compensate for the on-chip element fluctuations. Cascade connection of these ICs achieves complete limiting operation at 1.8GHz with small phase-shift deviation under 10 degrees over the input dynamic range from -42 to -14dBm. The results demonstrate the feasibility of monolithic integration of a timing circuit in very-high-capacity optical systems.

§1. Introduction
Recently, requirements of high-capacity communication systems have been steadily increasing. This has produced a strong requirement for monolithic amplifier ICs to achieve highly reliable, power efficient, compact communication systems.
Tuning and limiting functions are very fundamental in various communication systems including optical transmission and satellite communication systems. A resonant circuit consisting of L and C are essential to realizing a tuning amplifier. However, in monolithic ICs these elements are difficult to integrate on the same chip because of large manufacturing fluctuations and space factors. Still more, external elements can not be utilized to the GHz band due to difficulty in fine adjustment.
The limiting amplifier operation requires that phase shift variation between input and output signals be small over a wide dynamic range of input signal level. Gallium Arsenide IC technology is one alternative for realizing amplifiers that can operate at ultra high frequencies with small phase shift. However, problems such as low yield or insufficiency of gm for 50 ohm low line impedance systems remain.
A useful alternative is an improved Si-bipolar technology, SST 1). It yields a self-aligned sub-micron emitter stripe transistors of 17GHz-ft. Using the SST-process and new circuit technology, tuning and limiting amplifier ICs have been developed.
This paper describes the design and measured performance of these ICs.
§2. Circuit design
2.1 Tuning amplifier
Tuning frequency of on-chip resonant circuits deviates from designed values owing to fluctuations in inductance and capacitance. Thus, if discrete devices are used, fine adjustment of tuning frequency is needed. However, adjustment is very difficult because of the very small time constant. Further, there is the problem of tuning frequency deviation by physical shock.
Therefore, this design incorporated an external PIN diode chip to adjust tuning frequency electrically. The resonant circuit inductor was formed in a spiral pattern on the same chip as the amplifier circuit.
The tuning amplifier circuit configuration is shown in Fig. 1. The first stage is the tuning stage with LC resonant circuit. The second is the gain stage and the third is the wide band output matching stage to the 50 ohm line.
Simulated tuning characteristics and gain dependency against resonant capacitance C of the first tuning stage are shown in Fig. 2. Parastic capacitances of the on-chip inductor were considered as shown in Fig. 2. The decrease in gain is due to Q decrease for the overall tuning circuit containing transistor parastic elements. If
only the inductance value of \( L \) can be made larger. \( Q \) and gain will increase. However, since parastic resistance and capacitance of \( L \) increase at the same time, actual \( Q \) and gain cannot be improved. Still more, the chip area becomes larger. Considering the above conditions and variable capacitance value of PIN diode, \( L \) of resonant circuit was designed as a 1.62\( \text{nH} \) rectangle spiral coil. The number of turns is 4 and line width is 10 \( \mu \text{m} \). The second stage is a differential amplifier with a new adjustable peaking function to improve gain at high frequency. 2) The peaking circuit consists of \( Q_7, Q_8, Q_{11}, Q_{12}, R_{18}, R_{21} \) and \( R_{22} \). By controlling terminal voltage \( V_{pc} \), the base to emitter capacitances of \( Q_7 \) and \( Q_8 \) can be varied. This varies peaking capacitance of the amplifier so as to cause peaking in the high frequency region.

The third stage is a parallel feed back amplifier. Output impedance at low frequency is expressed by equation (1):

\[
R_{out} = \frac{R_{29} + (R_{24}/R_{25}/R_{inQ})}{1 + \beta(R_{24}/R_{25}/R_{inQ})} / R_{eq} \tag{1}
\]

where \( R_{inQ} \) is input impedance of \( Q_{27} \) or \( Q_{28} \), \( R_{eq} \) is output impedance of \( Q_{27} \) or \( Q_{28} \) and \( \beta \) is a common emitter circuit current gain of \( Q_{27} \) or \( Q_{28} \). Capacitors \( C_6 \) and \( C_7 \) were added to compensate for the output impedance increase in the high frequency region.

2.2 Limiting amplifier

A differential amplifier generally has many phase-shift mechanisms such as input voltage offset or unbalancing between differential outputs. 3) In this design, single-ended form was adopted for its small phase deviation.

Basic circuit configuration is shown in Fig. 3. The limiting characteristic is obtained as follows: When input voltage is low, \( Q_1 \) is OFF and \( Q_2 \) is ON. Therefore, output voltage is about 1 \( V_{be} \). At that time, \( Q_5 \) saturates, though there is no degradation of the ac characteristic. On the other hand, when input voltage is high, \( Q_1 \) is ON and \( Q_2 \) is OFF. Current flowing in \( R_2 \) is limited by \( Q_5 \) and output voltage is restricted to \( (V_{cc}-I\cdot R_2-V_{be}) \), where \( I \) is the current value of the current source consisting of \( Q_4, Q_5 \) and \( R_4 \).

Bias condition is very stable because \( Q_1 \) is biased in the active region near cut off by \( R_3 \) automatically. Voltage gain at low frequencies is expressed by equation (2), when diode resistance of \( Q_5 \) is nearly equal to 0:

\[
G_v = \frac{g_{m1}}{(1 + g_{m1} \cdot R_{sat})} \cdot \frac{R_1 \cdot (g_{m2} \cdot R_2 - 1)}{(1 + g_{m2} \cdot R_1)} \tag{2}
\]

where \( R_{sat} \) is C-E saturation resistance of \( Q_5 \) and \( g_{m1} \) and \( g_{m2} \) are transconductance of \( Q_1 \) and \( Q_2 \), respectively.

If \( R_{sat} = 0 \) and \( g_{m2} \cdot R_2 \geq 1 \), \( g_{m2} \cdot R_3 \geq 1 \), equation (2) is reduced to equation (3):

\[
G_v = g_{m1} \cdot R_2 \tag{3}
\]

The dc transfer characteristics calculated by varying \( R_1 \) as a parameter are shown in Fig. 4.

Fabricated circuit configuration of the limiting
amplifier which consists of 4 basic limiting stages and a distributor circuit is shown in Fig. 5. To achieve stable operation, the current source value was made to be adjustable by varying terminal voltage $V_B$. This current value is sensitive to stability.

2.3 Chip layout

Chip photographs of the tuning and the limiting amplifier ICs are shown in Fig. 6 and Fig. 7. A common GND and dc feeding lines were separated by stage to prevent a coupling for forming through these lines.

§3. Measured performances

3.1 Chip mounting

A ceramic plate for evaluation, on which the IC chip is mounted, is shown in Fig. 8. Ample isolation of the input and output is necessary for stable operation. For that purpose, lowering the impedance of dc supply line and reducing the coupling between input/output signal line are needed. Therefore, a grounded-co-planar line was used as the signal lines and a high-permittivity ceramic thin sheet of 500pF capacitance was used for dc feeding lines.

3.2 Performance

Frequency responses of $S_{21}$, $S_{11}$ and $S_{22}$ as well as tuning frequency controllability of the tuning amplifier are shown in Fig. 9. Tuning frequency can be varied over the $1.4 \sim 1.85$GHz range and 17dB gain was obtained at 1.8GHz.

Frequency responses of the limiting amplifier are shown in Fig. 10. Gain is 32dB at 1.8GHz.
Frequency responses of $S_{21}$, $S_{11}$ and $S_{22}$ and tuning frequency controllability of the tuning amplifier.

Phase-shift and limiting characteristics of the tunable limiting amplifier, measured at 1.8 GHz using these ICs are shown in Fig. 11. Complete limiting operation with very small phase-shift deviation under 10 degrees is achieved over the input dynamic range from -42 to -14 dBm. The output waveform is shown in Fig. 12.

Measured characteristics are summarized in Table-1.

4. Conclusion

A wide dynamic range from -42 to -14 dBm with very small phase-shift deviation under 10 degrees at 1.8 GHz has been achieved by two ICs. These ICs can be applied to very high capacity optical fiber transmission systems.

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References