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Si Bipolar Multi-Gbit/s Logic Family Using Super Self-Aligned Process Technology

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A Si bipolar multi-Gbit/s logic family with 50 ohm load driving capability is developed. To achieve high performance, Super Self-aligned process Technology (SST) is adopted. To optimize circuit parameters and transistor size, a highly accurate transistor model is constructed, which agrees well with measured f_T characteristics. New circuit configuration is introduced for multi-Gbit/s use. The family operates up to about 4 Gbit/s and is of sufficiently superior performance for a future optical fiber transmission system.

Introduction

The future very high-speed optical fiber transmission system and high-speed digital system will require very high-speed logic ICs operating up to the multi-Gbit/s level at performance. A Si bipolar technology is one of the most promising candidates from the perspective of high-speed and high driving capability with low power dissipation. In this paper we describe a Si bipolar multi-Gbit/s logic family with a 50 ohm load driving capability. The family consists of several kinds of ECL compatible logics (e.g. OR/NOR, D-F/F) and special logics for transmission systems (e.g. decision circuit). The family operates up to about 4 Gbit/s, which is achieved through the following three key technologies;
(1) Super Self-aligned process Technology (SST)[1],
(2) highly accurate transistor model, and
(3) new circuit configuration.

Process Technology

A cross-sectional view of an NPN transistor using the SST is illustrated in Fig.1. The fabrication process steps of the SST were already reported in reference (1). The main features of the SST are a minute transistor structure; a 0.5 μm wide-emitter, a 0.3 μm wide-base contact, and a 0.3 μm base-emitter space. Such a small emitter and external base region reduce base resistance and base-collector junction capacitance. Furthermore, the doped polysilicon technique makes it possible to form stable shallow junctions; a small base width of 0.07 μm is achieved. Consequently, a high cut-off frequency (f_T) of 12.3 GHz is obtained at V_{CE}= 3 V.

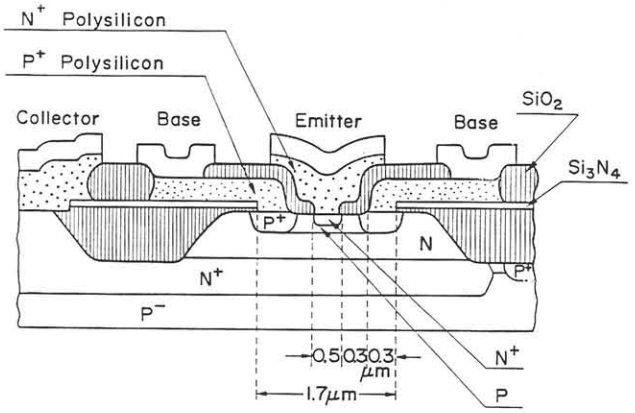

Fig.1 Cross-sectional view of NPN transistor using SST

Accurate Transistor Model

To predict circuit performance in the multi-Gbit/s region and to optimize circuit parameters and transistor size, a highly accurate transistor model should be constructed, which agrees well with measured f_T vs. collector current(Ic) characteristics over a wide Ic range.

For this purpose, it is important to determine whether or not the two-dimentional effect

is neglected for such a kind of submicron-emitter transistor. Then one- and two-dimensional device analysis is done to investigate f_T characteristics for the transistor structure of Fig.1, using the device simulator TRANAL[2]. The results are shown in Fig.2. The f_T peak values are obtained for 13 GHz at Ic=0.7 mA by two-dimensional analysis, and 19 GHz at Ic=1.15 mA by one-dimensional analysis, respectively. There is a significant difference. Thus, it is confirmed that the two-dimensional effect, the so-called emitter-crowding effect must be taken into account when fitting the f_T curve for even this minute transistor structure.

To represent the emitter-crowding effect, a new model (described in detail later) is introduced as a one-emitter finger transistor. As actually fabricated transistors have multi-emitter fingers, the entire model is constructed by arranging the model corresponding to a one-emitter finger in parallel. For example, five-emitter finger transistor model is shown in Fig.3, which has the following features.

(a) As the basic transistor(Qe) which corresponds to the one-emitter finger, is put in parallel with the collector buried layer resistance Rc(buried) and collector-substrate capacitance(C_{TS}), the correct bias condition of each basic transistor is expressed accurately.

(b) The Qe consists of intrinsic (Qint) and extrinsic (Qex) parts to express the emitter-crowding effect.

(c) The Qint and Qex are described by Gummel-Poon model which includes the high injection effect as well as the early effect.

To reduce the number of Gummel-Poon model parameters, the inverse high injection effect parameters in Qint and Qex are neglected, because for our purpose transistors should not be biased in the region where this effect occurs. Parameters are derived from two-dimensional analysis and measurements of transistor characteristics.

SPICE simulation results of this model are shown in Fig.4 in comparison with experimental results; f_T vs. Ic characteristics for V_{CE}= 1, and 3 V. Simulated results agree very well with experimental data.

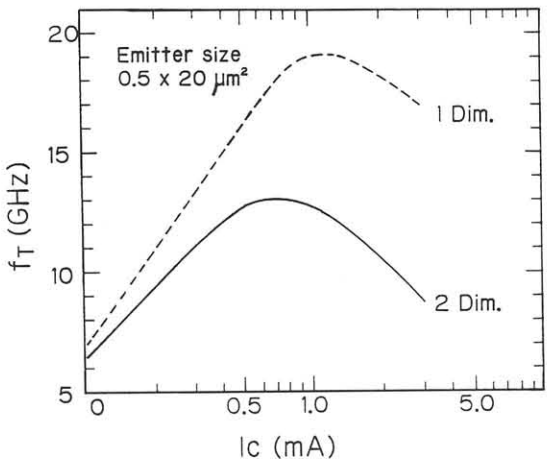

Fig.2 Cut-off frequency(f_T) vs. collector current (Ic) characteristics by using device simulation

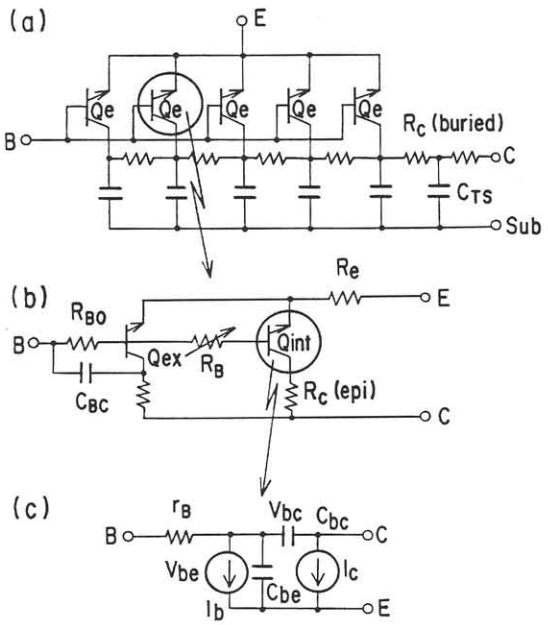

Fig.3 Five-emitter finger transistor model

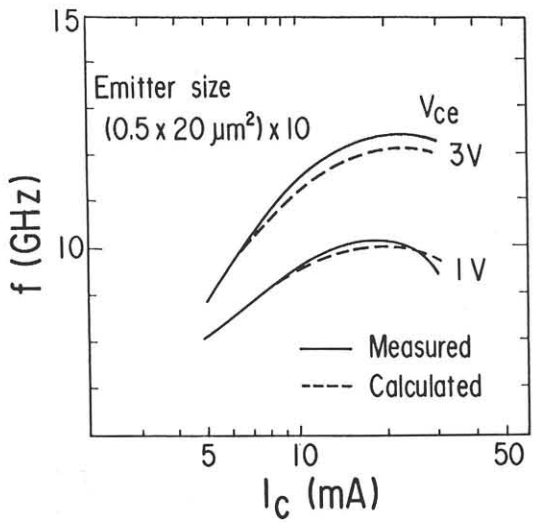

Fig.4 Simulated f_T characteristics compared with experimental data

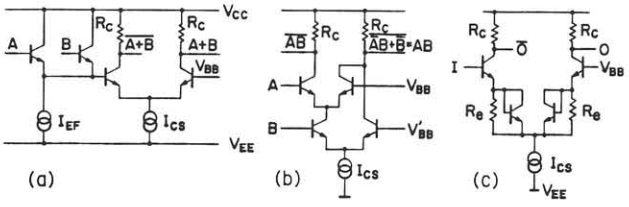

Fig.5 Three basic circuit techniques (a) E^2CL (b) series-gated ECL (c) modified NTL

Circuit Design

As basic circuit techniques, an E^2CL , a series-gated ECL and a modified NTL[3] are adopted. These circuits are shown in Fig.5.

(a) An E^2CL is used for 2 or 4 input OR/NOR circuits to minimize the Fan-In coefficient.

(b) An exclusive-OR/NOR, a decision circuit and flip-flops are constructed by a series-gated ECL structure to realize low power dissipation and high-speed operation.

(c) Futhermore, a modified NTL configuration is introduced, which was already described in detail in reference (3).

To obtain a faster transition time, open collector output devices are also fabricated in addition to conventional open emitter output devices for each function.

For a circuit design example, a new D-type master-slave flip-flop (F/F) configuration is shown in Fig.6, which consists of clock buffer (a) , master F/F (b), slave F/F (c), output buffer (d), and voltage supply parts. The difference between this circuit and a conventional ECL D-type master-slave F/F is the adoption of the clock and output buffers. Stable and fast circuit operation is achieved up to the multi-Gbit/s region by the following points.

(1) The utilization of differential driving for F/F switching by using a clock buffer.

(2) The reduction of internal logic swing to 450 mV in F/F.

(3) The adoption of a large switching current of 18 mA for the output buffer to reshape waveform and to assure a fast transition time.

The power dissipation of this chip is 525 mW and its size is 1 mm X 1.25 mm.

Characteristics of this IC family

The transition time (10 - 90%) obtained for several circuits are listed in Table 1. The tr

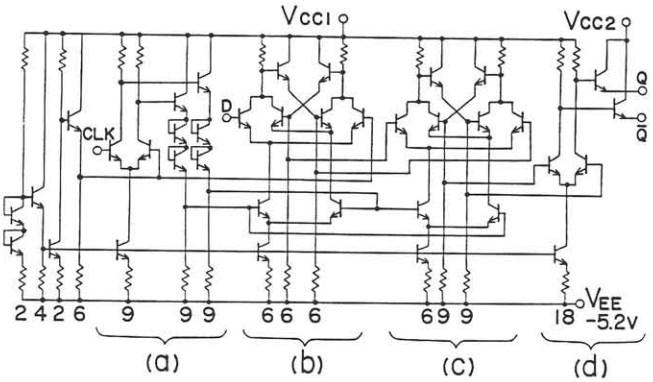

Fig.6 Circuit configuration of D-type master-slave flip-flop
(a)clock buffer (b)master flip-flop
(c)slave flip-flop (d)output buffer

Table 1 Measured transition time (10-90%) of the family at 2 GHz

Function	output type	tr (psec)	tf (psec)	power (mW)
2-in and 4-in OR/NOR gate	O.C.	130	130	229
	O.E.	150	100	229
EX-OR/NOR gate	O.C.	140	140	279
	O.E.	150	150	223
Level converter	O.C.	130	130	237
	O.E.	150	130	239
M-S F/F with Clk buf.	O.C.	90	90	588
	O.E.	150	150	525
M-S F/F with R,S	O.E.	150	150	510
Decision circuit	O.C.	90	90	608
1/8 Divider	O.E.	140	140	884

and tf are always less than 150 ps with an input of 2 GHz and a load of 50 ohm. For the F/F having open collector outputs, 90 ps is obtained. All devices are guaranteed to be error free up to 2 Gbit/s. This maximum error free operation bit-rate is limited by measurement tools. Concerning the maximum operating frequency, 5.5 GHz is obtained for a 1/8 divider. The waveform of a 1/8 divider at 5.5 GHz is shown in Fig.7.

Application

To verify the performance of the family, a 4-1 multiplex/ 1-4 demultiplex circuit is constructed using packaged chips. The logic diagram is shown in Fig.8. In the multiplexing part, 4 parallel input signals are selected by a 2-input NOR gate which is activated one after another by using a different phase clock signal with a 25%

duty ratio. These signals are multiplexed by the 4 input NOR gate, then the D-type master-slave F/F regenerates the 4 times faster serial signal. In the demultiplexing part, 4 D-type F/Fs are triggered one after another by using clock signals that are 1/4 speed. Then, the faster serial signal is demultiplexed to 4 original signals.

Figure. 9(a) shows the 3.2 Gbit/s multiplexed waveform for 800 Mbit/s pseudo-random data inputs, which have good eye-opening. A transition time of about 90 ps is obtained. These results indicate that the family is of sufficiently superior performance for the terminal equipment of a future optical fiber transmission system. Futhermore, the circuit can operate error free at up to 4 Gbit/s . This error free operation is confirmed by using demultiplexed data. The multiplexed waveform at 4 Gbit/s is shown in Fig.9(b), which has a good eye-opening. This guarantees an operation of 4 Gbit/s for this family.

Conclusion

A Si bipolar multi-Gbit/s logic family with 50 ohm load driving capability has been developed. To obtain high performance, a Super Self-aligned process Technology(SST) is adopted.

To predict circuit performance and to optmize circuit parameters and transistor size , a highly accurate transistor model is introduced.

Futhermore, the new circuit configuration is designed for multi-Gbit/s use.

The family operates at up to about 4 Gbit/s and will be applicable to a future optical fiber transmission system etc.

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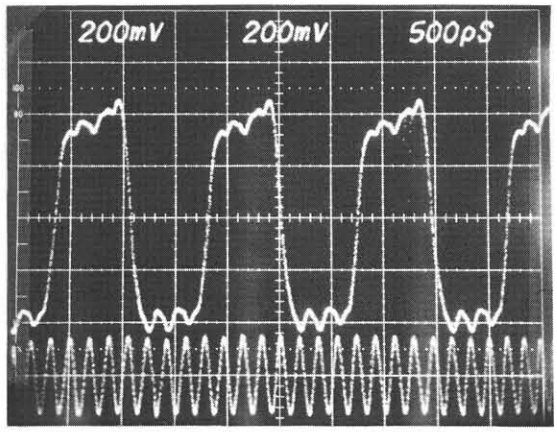


Fig.7 Waveform of a 1/8 divider at 5.5 GHz

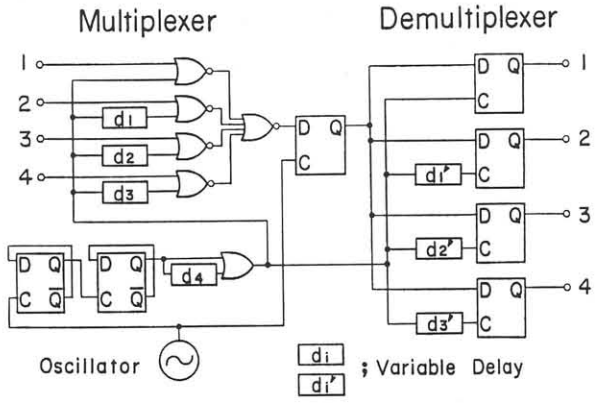
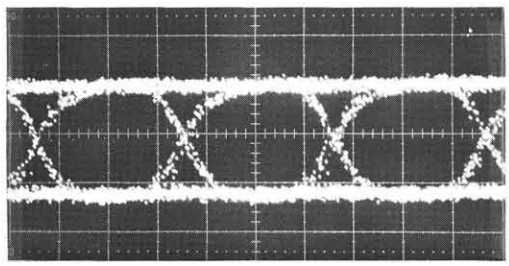
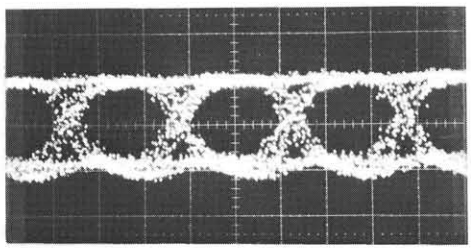


Fig.8 Logic diagram of a multi/demultiplexer using this family



(a) 3.2 Gbit/s V: 0.5 V/div H: 100 ps/div



(b) 4 Gbit/s V: 0.5 V/div H: 100 ps/div

Fig.9 Multiplexed waveforms