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Invited

Device and Materials Implications of VLSI's

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What VLSI's, or integration of very large number of components on silicon chips, imply in terms of devices and materials is discussed in an attempt to highlight several areas where further research and development efforts are needed for the next several years. The rapidly evolving performance trends of VLSI's are translated into sizes and properties required of constituent devices and materials. Which directions these requirements tell us to follow and how far is the subject of this article.

1. Introduction

Rapid progress in silicon integrated circuit technology over the past decade is probably one of the most remarkable in the history of human technological achievement. Integration of larger number of components per chip has made the systems more reliable, less costly, and faster. The information processing speed of the fastest computers has increased by a factor of 10 over the decade. Benefited even more directly from the progress of VLSI's are small systems based on micro- and mini-computers, where architecture is centered at the design and use of VLSI itself. These trends are shown in Figs. 1 and 2.

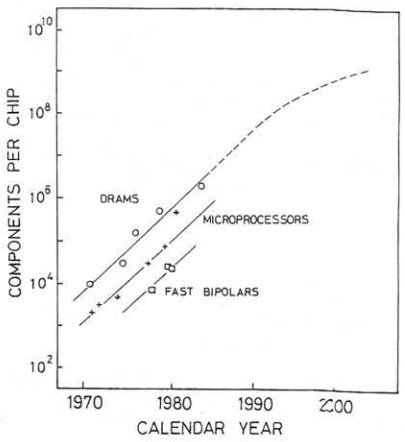

Fig. 1 Number of components per chip versus calendar year.

At the present time, we put more than half a million transistors and capacitors on a chip to build a 256 Kbit MOS dynamic random access memories. For this purpose, the industry is primarily using 2 μm lithography, polysilicon or silicide gate, 40 nm-thick gate oxide, and a single-level Al metallization. MOS microprocessor units with half a million transistors are also in production. MOS VLSI's with 2 million component counts will be mass-manufactured within a few years.

Predictions have been made as to how far this trend will continue (1). At the current rate, we will hit 10^8 components per chip by the mid 1990's. Memory capacity in excess of 2 MB, and a computing power more than 1 M gates will be available on a chip.

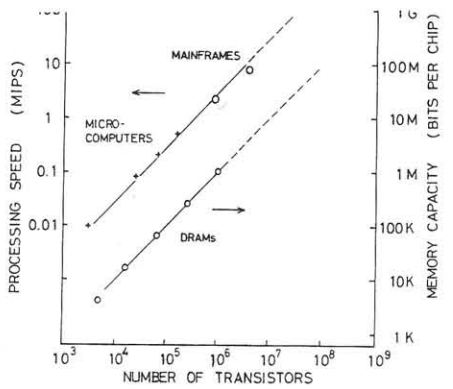

Fig. 2 Performace of VLSI's as a function of number of transistors.

What kind of devices and materials will we be using for the VLSI's of the 1990's with component counts on the order of 10^8 ? What type of work will be required to achieve it? In this paper, we shall address to these questions, and try to highlight problem areas where future work is needed.

2. Dynamic Memories

Memory Cells and Capacitor Dielectrics

A MOS DRAM memory cell consists of a storage capacitor and a switching transistor connected in series. The signal charge on the capacitor, representing the logical status, can therefore be stored only for a limited duration of time, on

the order of a second. It has to be refreshed from time to time, hence the name dynamic.

The storage capacitor has to be designed so that it is capable of storing enough charge, which ensures immunity to various causes of noise: minority carriers generated by alpha-particles and impact ionization, junction leakage, supply voltage variations, crosstalks, and fabrication tolerances. From the above consideration, the minimum signal charge required is,

$$Q_S \geq 2 \times 10^{-13} \quad C$$

whereas the total charge generated by a typical alpha is of the order of 1×10^{-13}C. What this means is shown in Fig.3(a). For the 64 K, the above charge was stored on a capacitor, 80 μm^2 in area, formed with a 40 nm-thick SiO_2, on which an electric field of about 1 MV/cm was applied. For the 256 K, the capacitor area was reduced to 40 μm^2, and the electric field had to be increased to 2 MV/cm, by employing a 20 nm-thick SiO_2, as dictated by the Gauss's law,

$$Q_S = \varepsilon A \quad E.$$

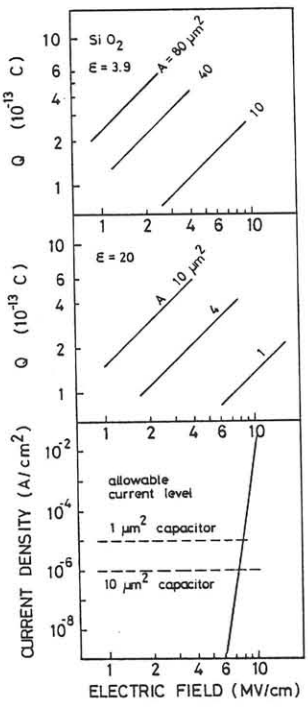

Fig. 3 Signal charge stored in capacitors with a dielectric constant of ε =3.9 (a) and ε = 20 (b).
Current density through an SiO_2 film is shown in (c).

If we assume a storage capacitor area of 10 μm^2 for the 1 Mbit, oxide thickness will have to be only 5 nm, and the electric field will be 8 MV/cm. Obviously, this is out of question, since the field is too close to the dielectric strength of SiO_2. Besides, at this thickness, current through the oxide will increase drastically due to direct tunneling.

One way to increase Q_S is to increase the effective capacitor area, A. The stacked capacitor and the corrugated capacitor (2) represent this approach, and the latter is particularly attractive for 1Mbit and beyond.

If, however, we had an insulator with a dielectric constant of ε = 20, e.g., Ta_2O_5, a lot lower field would suffice to store the required charge, as shown in Fig.3(b). We cannot be too optimistic here, however, since the dielectric constant of high-ε insulators is generally lower compared with SiO_2.
In the use of very thin, and/or new insulating materials for storage capacitor, the current through it can be another signal-charge loss mechanism. The allowable current density, J, is given by,

$$J \quad A \quad t_{ref} << \frac{1}{2} Q_S,$$

where the refresh cycle time, t_{ref} is usually chosen to be 2 ms.
For a storage area of 10 to 1 μm^2 and with a margin of a factor of 100,

$$J = 10^{-5} \sim 10^{-6} \ A^{-2}cm,$$

which can be regarded as breakdown criterion of insulators for a DRAM capacitor. This is illustrated in Fig.3(c) along with the current measured in thermally grown SiO_2.
More practical criteria could be set considering the reliability of the insulator as revealed by the TDDB (time-dependent dielectric breakdown) experiment. Search for new insulating materials with good dielectric properties and Si-process compatibility is definitely a challenge set by future DRAMs.

Word-Line Delay

In certain DRAM cell arrays, the switching MOS gate is directly used as the word line. In this case, the RC delay due to the gate resistance can make a significant contribution to the access time of the memory. Doped poly-silicon gate, has a rather high sheet resistance of 30 $\Omega/\square$. If we assume a floating capacitance of 1 pF/1000 $\square$, the line-delay can amount to 30 ns/1000$\square$, as shown in Fig.5. This can be very serious for the design of DRAMs with an access time of the order of 100 ns. Silicide gates, or more exactly, refractory metal silicides (WSi_2, $MoSi_2$, $TiSi_2$ and $TaSi_2$) on top of poly-silicon, have proven to be a viable technology, with a sheet resistance of 2 - 5 $\Omega/\square$. This has made possible a fast, noise-immune, closed-bit-line cell array, which requires a long word line.

Because the use of low-resistivity gate is thus associated with the memory mat structure, decrease in resistance by a factor of 4 or more will have a significant impact. The next step of lowering the gate resistance is therefore targeted at below 0.5 $\Omega/\square$, which inevitably leads us to pure refractory metals like W and Mo. This would result in a delay time two orders of magnitude smaller than with poly-silicon gate, as shown in Fig.4.

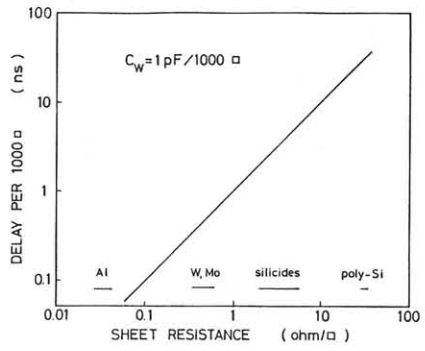

Fig. 4 RC delay time for various MOS gate materials.

There has been a lot of work aimed at the use of pure refractory metals for MOS gate. The most formidable obstacle has been the corrosion of these materials during the process, especially in oxidizing ambients. The recent report on the annealing of Si wafers with W gate in wet hydrogen seems to be a gateway to the solution: This new process slightly reoxidize silicon while W is kept intact, or rather, reduced (3).

Purification of Mo and W sputtering targets is on its way. CVD, or deposition of these metals by chemical reaction of vapor is also being pursued. The chemical, electrical, and mechanical properties of refractory metals, especially at interface with Si, SiO_2, and other metals are very important and worth extensive future studies. With pure refractory gates in hand, the design of fast DRAMs as well as SRAMs beyond 1 Mbit will be facilitated to a great extent.

3. Logic VLSI's

MOSFET Breakdown Voltage and Hot-Carrier Effects

One of the big concerns at the moment is if VLSI's with gate lengths below 1.5 μm can be safely operated at 5 V. This is important, since the systems world is currently standardized at this voltage.

The problem is easily understood by looking at the I-V characteristics of conventional MOSFETs with As source and drain in the gate lengths range of present interest. The breakdown voltage is already 7 - 8 V at the gate length of 1.3 μm. The minimum drain breakdown voltage, $minBV_{DS}$, is plotted against gate length in Fig.5. The gate oxide thickness is properly scaled in this experiment.

A constraint on the MOSFET operational conditions severer than the breakdown is set by the hot-carrier effects: energetic electrons or holes injected into the gate oxide generate fixed charge, which cause deterioration in gain and threshold shift (4). The maximum drain voltage for safe operation over the period of 10 years estimated from an accelerated test is shown in Fig.5 as "hot-carrier resistance." It is seen that operation of MOSVLSI's at 5 V is already marginal at the gate length of 1.5 μm.

Two approaches have been made to cope with this problem. The first approach is to tailor the drain impurity distribution so as to lower the electric field which gives rise to hot carriers. As-P double-diffused drain (DDD) and lightly doped drain (LDD) are among the structures proposed for this purpose. Their structures, as well as their breakdown voltages are shown in Fig.5.

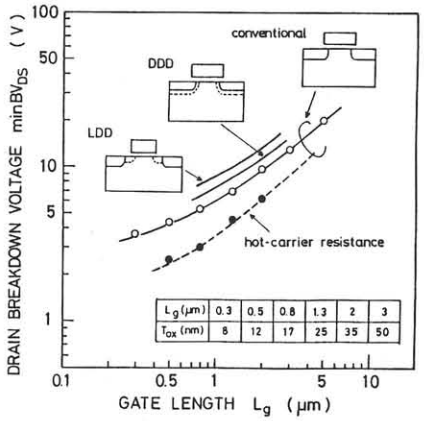

Fig. 5 Drain breakdown voltage and hot-carrier resistance as functions of MOS gate length.

A considerable increase in the breakdown voltage has been achieved with the LDD structure. Since it has series resistances at its source and drain, however, the increase in minBVDS is accompanied by a decrease in drain current. The trade-off is made by varying the length, depth and doping concentration of the lightly doped drain.

The second approach is to look for gate insulators less subjective to hot carriers, which is now being extensively pursued.

At present, it is unlikely that we will have to switch the supply voltage from 5 V at 1.3 μm. However, it is obvious that a new voltage standard below 5 V must be adopted for submicron MOS VLSI's. No matter what it is going to be, we are kept challenged by the lowering breakdown voltage and increasingly severe hot-carrier effects.

Multi-Level Wiring

Probably more peculiar to logic VLSI's is the need for multi-level wiring. It comes from requirements for shorter delay time and smaller chip area, and these two are closely related to each other. We shall begin by considering the chip area first.

In modern VLSI logic chips carrying tens of thousands of gates, a sizeable portion of the chip area is used up for aluminum wiring only. It is therefore worth while to consider in a crude model how the chip area can be saved by multi-level wiring.

The total length of wiring required to provide interconnection between gates has been estimated to be (5)

$$l_T = \frac{4}{3}\sqrt{A/B}\ (B^{1/6} - 1)\ Np,$$

where A is the area to be wired (chip area minus area required for external drivers and bonding pads), B is the number of blocks into which logic functions are modularized, and Np is the total number of signal pins these blocks have. Both B and Np are directly proportional to the total number of gates, G, on the chip.
With n levels of wiring,

$$n A = K p^2 G + 2 l_T p,$$

where p is the pitch of wiring. It is assumed by an empirical rule that a gate occupies an area of $K p^2$, and that 50 % of wiring is utilized.

These coupled equations are easily solved to yield A as a function of G. The results are shown in Fig.6 with n as a parameter. It can be seen that a considerable saving in area can be achieved by multi-level wiring.

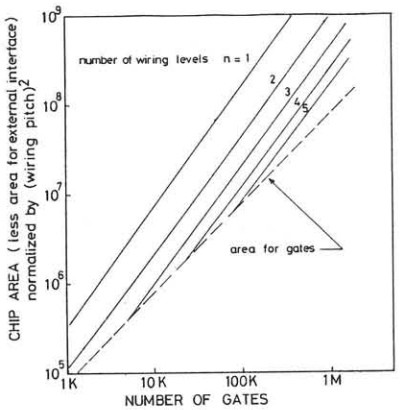

Fig. 6 VLSI chip area less output area as a function of number of gates.

Multi-level wiring is where new materials, and new processes are called for. Inter-level insulators, both inorganic and organic, and interconnect metals, both aluminum-, and refractory-based, are being extensively investigated. Damage-free, and self-planarizing processes are badly needed. In this respect, polymides, e.g, PIQ, as insulators and CVD metals are of great interest.

The delay time in an LSI is expressed as (6)

$$t_d = t_{do} + \Delta t_d C_{in} f_o + \Delta t_d C_w$$

where t_{do} is the intrinsic circuit delay, C_{in} the gate input capacitance, f_o the fanout, and C the wiring capacitance. In highly integrated MOS VLSI's, one has to be particularly careful about the wiring delay. Since C_w is directly proportional to the wire length,

$$l_w \propto \sqrt{A},$$

reducing the chip area by the use of multi-level wiring is also critical for increasing the circuit speed.

The inverse load driving capability, Δt_d is expressed as,

$$\Delta t_d = \frac{1}{g} + R_W,$$

where g is the conductance of circuit driver, and R_W is the wiring resistance. It is desirable to make g as large as possible, but not to exceed $1/R_W$. Use of bipolar drivers in MOS circuitry is very attractive in this regard.

4. Discussions

The level of integration forecast in Fig. 1 will only be realized as the consequence of future progress in fine-line patterning technology as predicted in Fig. 9. This will call for a great deal of research efforts to be put in on materials for lithography and dry etching. Resists of all kinds, membranes for X-ray masks, and gases for dry etching are only a few examples.

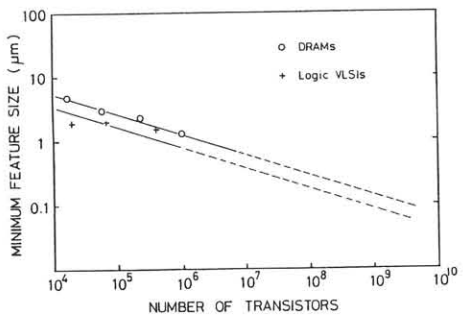

Fig. 7 Mimimum feature size required to achieve VLSI's

Since active devices as small as 0.1 μm have proven to work, there is no fundamental limitations up to the point where we might possibly integrate more than 108 devices per chip. Probably one of the biggest remaining issue then will be how to dissipate the heat.

As the heat and current densities go up, how to prevent interdiffusion and migration of materials will also become a great concern. Studies of interfaces of all kinds, between silicon, metals and insulators will be of primary importance. Very high integrity of materials and interface is required, and it will be achieved only by high-quality, defect-free, and damage-free processes.

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