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A 0.85 ns 1Kb Bipolar ECL RAM

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A 1Kb ECL RAM with an address access time of 0.85 ns and a power dissipation of 950 mW has been developed. Such performance is achieved using SST technology with 1 μm rule and high speed circuit design. The emitter width of the transistor is 0.5 μm and the cutoff frequency is 12.4 GHz at V_{CE} = 3 V. The minimum metallization pitch is 3 μm in the first layer and 6 μm in the second layer.

1. Introduction

A high speed 1Kb ECL RAM with an address access time of 0.85 ns has been achieved using Si bipolar technology. This paper describes the circuit design, process technology and performance of this RAM.

The key technology used in achieving such a high speed RAM is SST[1][2] (Super Self-aligned process Technology) with 1 μm rule. SST provides transistors with very low parasitics and a high cutoff frequency.

High speed circuit design is also used in the RAM. Previously, an address access time of 1.5 ns was achieved using this RAM circuit design and another type of SST with 2 μm rule[3][4]. In this work, an address access time is improved 40% by combining SST and high speed circuit design.

2. Circuit Design

Figure 1 is a block diagram of a 256W x 4b RAM. The 32 x 32 cells are arranged in four blocks, each with 32 rows and 4 columns. This arrangement minimizes chip size, interconnections and access time. Internal delays in this RAM are also shown in Figure 1. They are simulated values using a circuit simulator, SPICE2, and measured transistor parameters.

The memory cell circuit, illustrated in Figure 2, is a conventional type except that the capacitance of the SBD (Schottky Barrier Diode) is used as a speed-up capacitor. The read

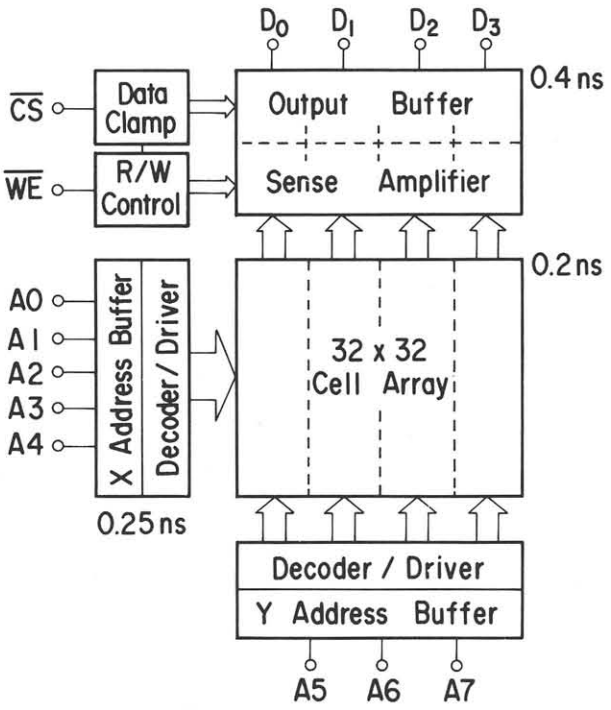


Fig.1. Block diagram of the 256 x 4 bit RAM and internal delays simulated using SPICE2.

current is 1 mA and standby current is 50 μA. The load resistor is 6 KΩ. Voltage swings between the two collectors in the memory cell are 300 mV in the standby cell and 500 mV in the selected cell.

The simplified RAM circuit is illustrated in Figure 3. In the address buffer circuit, the reference voltage (at point B) changes in the direction opposite to the input signal (at point A) only during the transition period. This is shown by the circle in Figure 3.

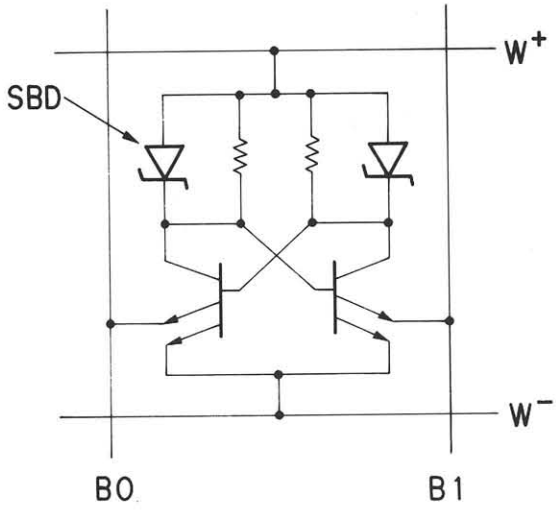


Fig.2. Memory cell circuit.

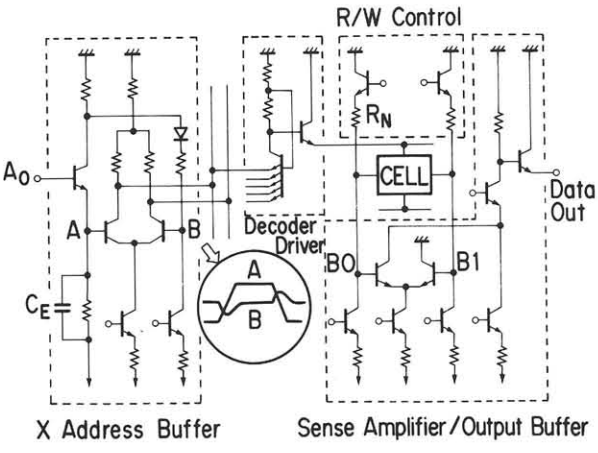


Fig.3. Simplified RAM circuit.

In the memory cell, C_{SBD}/C_{TS} is increased to achieve fast response of the collector voltage. C_{SBD} is the junction capacitance of the SBD and C_{TS} is the parasitic capacitance between the collector and the substrate.

In the sense amplifier, the differential voltage between the bit lines are compared and amplified at the same stage. Since the read current is 1 mA, it can directly drive the CML gate to produce a 4 mA flow. This current is converted into a voltage signal with an ECL level in the output buffer circuit.

These three circuit techniques bring about 50% improvement in the address access time compared with its predecessor.

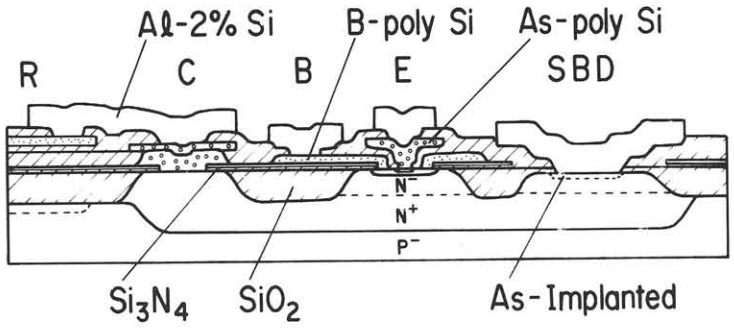


Fig.4. Cross section of the memory cell.

Table 1. Parameters for a transistor with 1 mA collector current.

Emitter size		$0.5 \times 8\ \mu m^2$
Cutoff frequency(*)	f_T	12.4 GHz
Base resistance	r_b	388 Ω
Collector-substrate capacitance	C_{cs}	42 fF
Collector-base capacitance	C_{cb}	18 fF
Emitter-base capacitance	C_{eb}	15 fF

(*) at V_{CE} = 3V

3. Process Technology

In order to achieve high speed access, SST with 1 μm rule is used. SST needs no mask alignment margin for fabrication of the transistor active region. In addition, it can realize an active region with a smaller feature size than a pattern made from photolithography. In this RAM, a 0.5 μm wide emitter and a less-than-2μm base region were fabricated from a 2 μm mask pattern. Therefore parasitic capacitances and resistances in transistors using SST are very low.

Moreover, the process temperature is relatively low after boron ion implantation in the base region and poly Si is used as the emitter diffusion source. This makes very shallow junctions, so a cutoff frequency of 12.4 GHz at V_{CE} = 3 V is achieved.

A cross section of a memory cell is shown in Figure 4. The parameters for a transistor using SST are listed in Table 1. The optimum collector current in this transistor is 1 mA. Some process parameters are listed in Table 2.

In the isolation process, planarized oxidation, called SPOT (Self-aligned Planar Oxidation Technology)[5] is used. This produces low parasitic capacitance and a flat surface.

Table 2. Process parameters.

Substrate (p type)	30 Ω·cm
Buried layer	As, 25 Ω/□
Epitaxial layer (n type)	0.5 Ω·cm, 1.1 μm
First metal	Al-2%Si, 0.8 μm
Interlayer insulator	P-CVD SiN_X, 1.2 μm
Second metal	Al, 1.5 μm

The resistors are made of poly Si. One uses arsenic-ion-implanted poly Si, which is the same as the doping source for the emitter. This resistor has a sheet resistance of 100 Ω/□ and 2 μm width. The other uses boron-ion-implanted poly Si, which is used in the memory cell and the standby current source. This resistor has a sheet resistance of 600 Ω/□ and 1.5 μm width. The 6 KΩ load resistor in the memory cell is realized in an area of 1.5 x 15 μm^2.

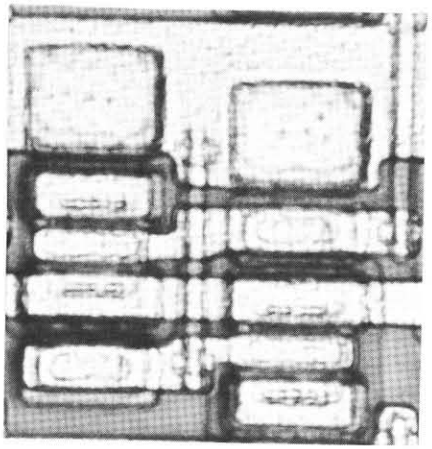
The capacitor has a Metal (1st layer) - Insulator (plasma CVD SiN_X) - Metal (2nd layer) structure.[6] The thickness of the interlayer SiN_X is 0.2 μm. This provides a 0.31 $fF/\mu m^2$ capacitance and high breakdown voltage (~80V). This type of capacitor has low series resistance and is suitable for use in high speed LSIs.

The SBD metal is Al-2%Si. In order to reduce the barrier height of the SBD, the Si region is implanted with arsenic. This increases the C_{SBD} which is used as a speed-up capacitor. The contact area is 4.5 x 7 μm^2 and the voltage drop at 1 mA (read current) is about 550 mV.

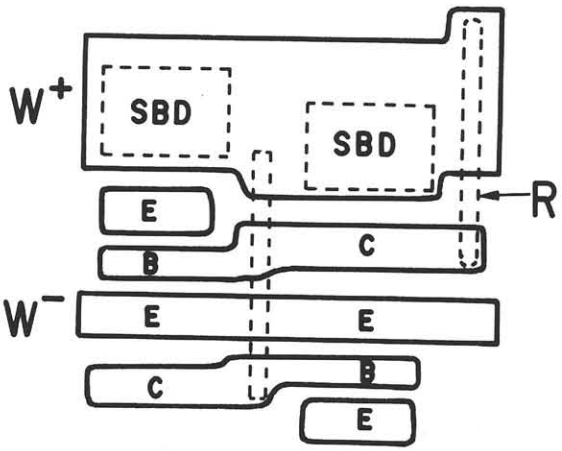
The first metal layer, the interlayer insulator and the second metal layer are Al-2%Si (0.8 μm thickness), plasma CVD SiN_X (1.2 μm) and Al (1.5 μm), respectively.

The minimum pitch of the first and second metal layers is 3 μm and 6 μm, respectively. In first layer metallization, three layer resist with amorphous Si[7] as the anti-reflective interlayer is used to fabricate the fine pattern. In second layer metallization, planarization and reflection suppression are used.

Microphotographs of the memory cell and the RAM chip are shown in Figures 5 and 6. The memory cell size is 32 x 32.75 μm^2 and the chip is 2.5 x 2.5 mm^2.



(a)



(b)

Fig.5. (a) Microphotograph and (b) top view of the memory cell.

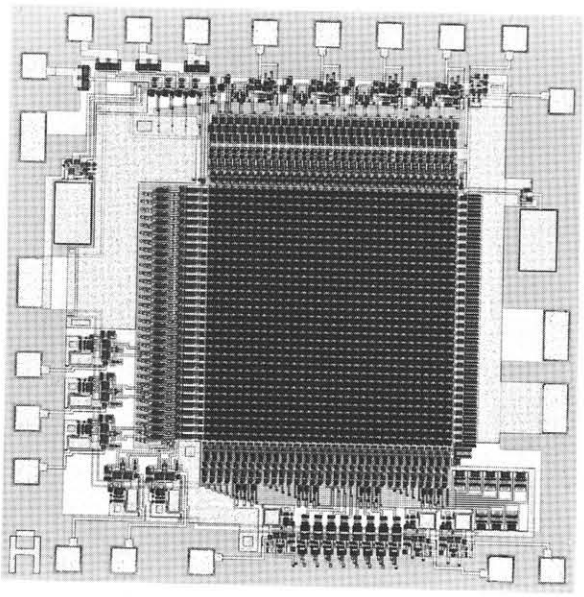


Fig.6. Microphotograph of the RAM.

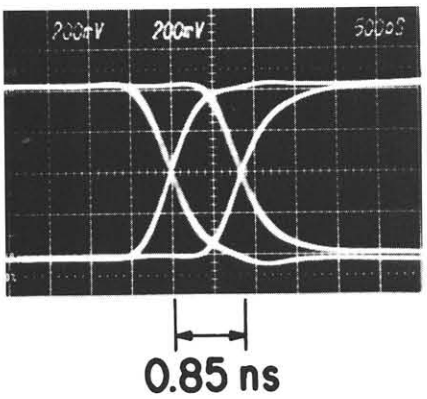


Fig.7. Address input and data output waveforms.

4. Performance

Figure 7 shows the input and output waveforms for the RAM. As shown, an address access time of 0.85 ns with 950 mW power dissipation is achieved. This agrees well with simulated values using SPICE2 and the measured transistor parameters.

The chip select access time is 0.65 ns and the minimum write pulse width is less than 1.5 ns. The power distribution and the performance of the 1 Kb RAM are listed in Table 3 and 4, respectively.

Table 3. RAM power distribution.

X decoder	220	mW
Y decoder	75	mW
Bit driver	235	mW
Cell array	174	mW
R/W control	93	mW
Sense amplifier	120	mW
V_R generator	33	mW
Total	950	mW

Table 4. RAM performance.

Organization	256 W x 4 b
I/O level	ECL
Power dissipation	950 mW
Address access time	0.85 ns
Chip select access time	0.65 ns
Write pulse width	$<$ 1.5 ns
Cell size	1048 μm^2
Chip size	2.5 x 2.5 mm^2
Power supply	-3.3V, -5.2V

5. Conclusion

A high performance 1Kb ECL RAM has been achieved by combining SST with 1 μm rule and high speed circuit design. Address access time for the RAM is 0.85 ns and the power dissipation is 950 mW. This RAM is applicable to cash memories for high speed computers and high speed digital switching systems.

Acknowledgement

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