Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 229-232

A-5-3

ABC — An Advanced Bipolar-CMOS VLSI Technology

Y. Okada, K. Kaneko, S. Kudoh*, K. Yamazaki* and T. Okabe

Central Research Laboratory, Hitachi Ltd.,
Kokubunji, Tokyo 185, Japan
* Takasaki Works, Hitachi Ltd.,
Takasaki, Gunma 370-11, Japan

A novel Bi-CMOS technology is proposed. Bipolar transistors (npn, pnp, I^2L) and MOS transistors (both n and p channel) have been successfully fabricated on the same chip with no decrease in performance. Shallow epitaxial layer($\lesssim 2\ \mu m$) is used in order to obtain small size and high performance(3 GHz) bipolar devices. Device sizes are reduced by using shallow junction and self-aligning technique. n-channel MOS transistors are formed in p-well regions designed to reach p-type substrate and p-channel MOS transistors are formed in epitaxial layer with n^+ buried layer. This technology has the potential for monolithic multi-functional analog/digital VLSI.

1. Introduction

Recent LSIs have required the integration of higher numbers of gates and elements. This makes the scale down of devices indispensable. Conversely, it has been considered advantageous to integrate various kinds of functions on the same ship [1]. Especially in the case of consumer products or the communication field, it is necessary to develop technology which can deal with both analog functions (amplifiers, filters, etc.) and digital functions (memories, processors, etc.). In answer to this request, fabrication of both bipolar and MOS devices on the same chip is highly desired because of their respective merits.

Several approaches have been introduced for such special applications as controllers, gate arrays and static RAM's. The conventional Bi-MOS technologies, however, have several limitations. For instance, the performance of bipolar devices fabricated in the CMOS process is poor. In other technologies, only common collector npn transistors can be fabricated [2]. In some technologies, npn transistors have wide base widths and large collector resistances which deteriorate performance [3] [4]. Furthermore, straight-forward processing for both bipolar and MOS transistors becomes more than doubly complex. These problems have limited further expansion of the application of Bi-MOS technologies.

In this report, a novel Bi-CMOS technology, ABC (Advanced Bipolar-CMOS) is proposed. This technology satisfactorily meets almost all the requirements of the analog and/or digital VLSI world.

2. Device structures and key techniques

The principal schematic cross-section utilized in this technology is shown in Fig.1. All devices, both bipolar and MOS transistors, are fabricated on the same chip. I^2L which consists of npn and pnp transistor can be also integrated.

This technology has the following specific features.

(1) n^+ buried layer

n^+ buried layer is used in order to reduce the collector series resistances of npn transistors and body resistances of p-channel MOS transistors.

(2) p-well region

n-channel MOS transistors are formed in p-well regions which reach p-type substrate. Because of this configuration, deep p-well which is used in the conventional CMOS process in

order to avoid latch up phenomena is not required. In this technology, thin epitaxial layer (≤ 2 μm) can be used, which reduces the gate sizes of bipolar transistors.

(3) Self-aligning technique

Self-aligning technique is used for the separation between the first and the second interconnections. The first interconnections are covered with SiO_2. Then it is etched away using dry etching method in such a way as side wall SiO_2 is not removed. This technique results in high performance bipolar devices due to the decreased parasitic areas. The distance between the emitter edge and base contact is determined by mask alignment and is designed to keep emitter region away from base contact in order to avoid leak current between base and emitter. A SEM photograph of this structure is shown in Fig.2.

(4) Common process steps

In order to simplify the process sequence or cut down the number of additional masks, some process steps are used in common. The same interconnection layer is used for bipolar and MOS transistors. The graft base of npn transistors and source or drain of p-channel MOS transistors are formed in the same step. By optimizing the impurity doping, inverse npn transistors in I^2Ls have been fabricated in the same process steps as normal npn transistors.

3. Results

Using 3 μm design rule, all devices have been experimentally fabricated. Typical emitter size is $3 \times 3\ \mu m^2$ and the gate length of MOS transistors is 3 μm. The thickness of the gate oxide is 50 nm.

(1) Bipolar transistors

Current gain h_{FE} (β_i for I^2L) and break-down voltage BV_{CEO} are the most important parameters. In order that I^2L devices have the same impurity profile as normal npn transistors, base Gummel number or active base impurity dose must be optimized. The dependence of current gain and BV_{CEO} on the base implantation is shown in Fig.3. For a dose of $8 \times 10^{13}\ cm^{-2}$, good performance is obtained. Current gain is independent of collector current below to 10^{-8}A. This means there isn't significant recombination current in the emitter-base junction. Typical I_C-V_{CE} curves of npn transistor are shown in Fig.4(a).

Gain-bandwidth product, f_T, of npn transistor is about 3 GHz. There are three reasons for this high performance: 1) the reduced collector resistance using n^+ buried layer, 2) relatively thin base thickness (0.3 μm) compared with conventional Bi-MOS technology, 3) the reduced transistor size due to self-aligning technique. The comparison of this technology with conventional Bi-MOS technologies is shown in Fig.5. Only isolated npn transistors (not including common collector configuration) are compared in this figure. Gate lengths show rough technology levels. The ABC technology has advanced f_T as much as five times compared with conventional results.

The minimum delay time of I^2L gate is about 5 ns and the propagation-delay time product is about 30 fJ at 1 μA/gate. The toggle frequency of a T-type flip-flop(TFF) is shown in Fig.6 as a function of injector current. Maximum toggle frequencies are 30 MHz.

(2) MOS transistors

3 μm gate length MOS transistors have been fabricated in this technology. The devices show reasonable performance. In the case of L=3 μm and W=10 μm, the threshold voltage V_{th}=0.7 V and the mutual conductance β =160 μS/V for n-channel transistor, and V_{th}=-1.6 V, β =40 μS/V for p-channel transistor. Transistor symmetry will be easily achieved by introducing the additional implantation step. Typical I_D-V_{DS} curves of n-channel MOS transistor is shown in Fig.4(b).

The important device dimensions and the typical device parameter values for this process are summarized in Table 1. All devices have good performance. Comparison of this technology with other conventional technologies is shown in Table 2. Conventional technology which is based on bipolar process has poor MOS characteristics, especially β, because of thick gate oxide. It is impossible to integrate pnp and I^2L using conventional technology based on MOS process.

4. Conclusion

A novel Bi-CMOS technology, ABC (Advanced Bipolar- CMOS) has been developed. This technology satisfactorily meets almost all the requirements of the analog and/or digital VLSI world:

(1) device sizes are reduced by using self-aligning technique and shallow junctions, (2) both high input impedance and high output current are available, (3) high frequency analog circuits, I^2L circuits, and low power MOS memories can be integrated on the same chip.

This technology has the potential of further expansion and wide application for the monolithic multi-functional analog/digital VLSI.

Acknowlegment

The authors wish to express their sincere thanks to Drs. M. Nagata, T. Nakamura and T. Watanabe at Central Research Laboratory and S. Ogura at Takasaki Works, Hitachi, Ltd. for their valuable discussions and encouragement.

References

(1) G. Zimmer et al:IEEE Trans. Electron Devices, vol.ED-26, pp.390-395 Apr. 1979

(2) P. A. Sullivan et al:IEEE Trans. Electron Devices, vol.ED-29 p.1679 Oct. 1982

(3) H. Momose et al:Proc. Symp. VLSI Tech. paper, p.40, 1983

(4) C. S. Yue et al:IEEE Electron Device Letters, vol.EDL-4, pp.294-296 Aug. 1983

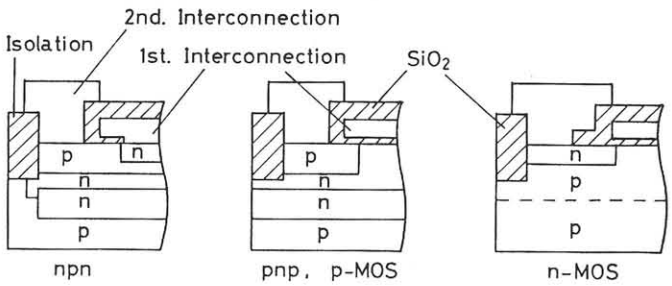


Fig.1 Schematic cross-section of proposed Bi-MOS device structures

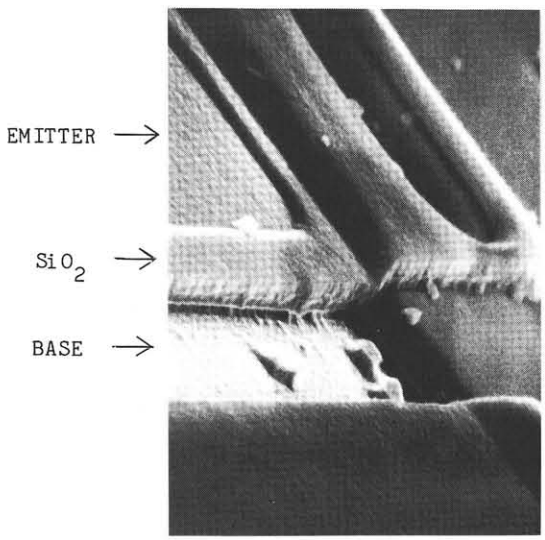
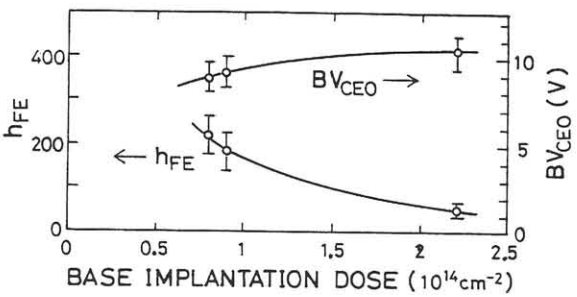
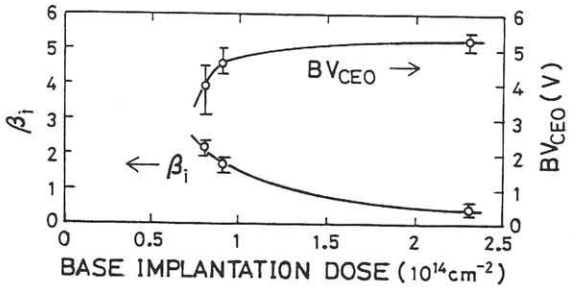


Fig.2 SEM photograph of npn transistor

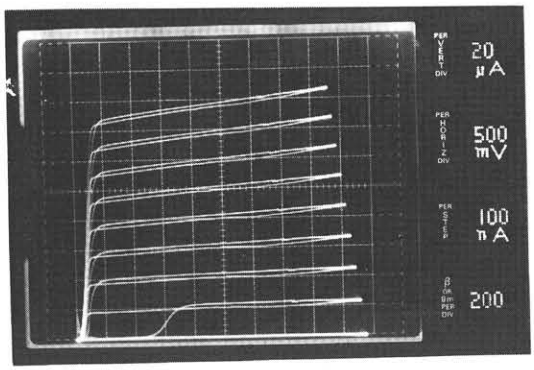


(a) normal npn transistor

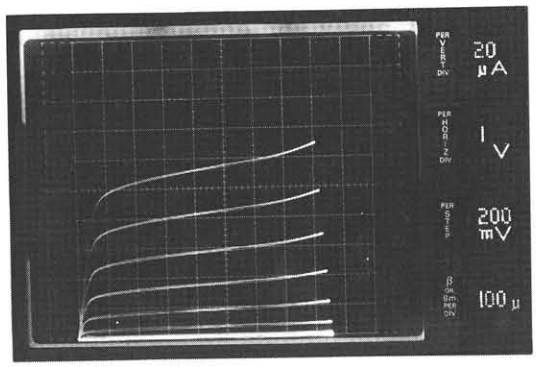


(b) inverse npn transistor

Fig.3 Dependence of current gain and breakdown voltage on base implantation dose



(a) npn transistor
(3 μm sq. emitter)



(b) n-channel MOS transistor
(L=3 μm, W=10 μm)

Fig.4 Typical I-V characteristics

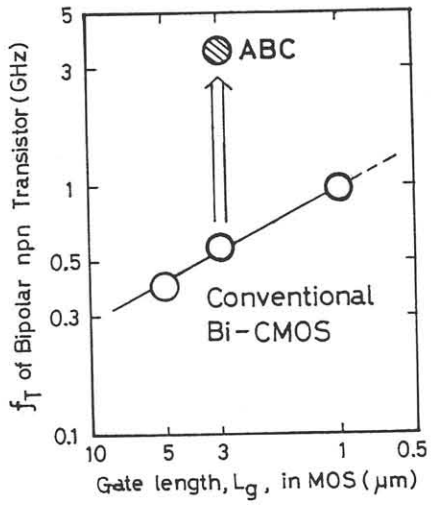


Fig.5 Comparison of gain-bandwidth product f_T
(only isolated npn transistors)

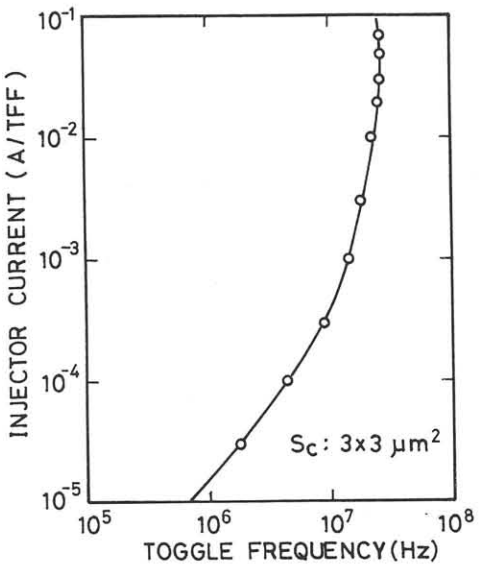


Fig.6 Toggle frequency vs. injector current for a T-type flip-flop

Table 1 Parameters of bipolar and MOS transistors

npn	emitter size	3x3 μm²
	h_{FE}	200
	BV_{CEO}	8 V
	BV_{CBO}	26 V
	f_T	3 GHz
	V_A	25 V
pnp	base width	3 μm
	h_{FE}	200
	BV_{CEO}	14 V
	f_T	50 MHz

I^2L	collector size	3x3 μm²
	$t_{pd\,min}$	5 ns
	$P_d \cdot t_{pd}$	30 fJ
n MOS	L_g	3 μm
	V_{th}	0.7 V
	BV_{DS}	20 V
	β	160 μS/V
p MOS	L_g	3 μm
	V_{th}	1.6 V
	BV_{DS}	20 V
	β	40 μS/V

Table 2 Comparison of device performance in Bi-MOS technology

Process \ Device	Bipolar			MOS		comment
	npn	pnp	I^2L	n-ch	p-ch	
conventional based on Bip.	○	○	×	△	△	poor MOS (β)
conventional based on MOS	△	×	×	○	○	poor Bip. (f_T)
ABC	○	○	○	○	○	excellent

○ : good △ : poor × : impossible