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Low-Power, High-Speed Bi CMOS Memory Circuits

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Abstract

This paper describes newly proposed BiCMOS memory circuits that make realization of a static RAM with a power-access product less than half that for conventional CMOS or bipolar memory circuits. By simulation and experiment, it is shown that the combined BiCMOS memory circuits consisting of a new memory cell and a new driver circuit have the advantages of incorporating both the low-power characteristics of CMOS circuits and the high-speed characteristics of bipolar circuits.

1. Introduction

Many intensive efforts have been made to achieve low-power, high-speed, high-density static RAMs. Up to now, great emphasis has been placed mainly on high speed for bipolar RAMs, whereas high density and low power dissipation were the objectives for MOS RAMs. Hence, RAMs that incorporate both the low-power characteristics of CMOS RAMs and the high-speed characteristics of bipolar RAMs are strongly desired.[1) 2)]

Under such circumstances, BiCMOS circuits composed of bipolar transistors (Trs) and MOS FETs are quite attractive. In general BiCMOS circuits, the MOS FETs control the bases of the bipolar Trs, which in turn drive the capacitive load, but no steady current flows. Therefore, the respective demerits of MOS FET and bipolar Tr are complemented. In spite of this advantage, few applications of BiCMOS circuits to RAMs have been reported.[3)] Hence, a new BiCMOS memory cell and a new BiCMOS driver circuit are proposed. Evaluation of these new circuits, using a small scale memory test chip, shows sufficiently stable memory operation and high performance. Then, these BiCMOS circuits prove to be useful in low-power, high-speed, high-density static RAMs.

2. BiCMOS memory circuits

As described above, BiCMOS circuits are generally expected to exhibit both low-power and high-speed characteristics. These excellent characteristics are utilized in the new memory cell and the new driver circuit proposed in this paper. This section describes the operational principles and the remarkable characteristics of these BiCMOS memory circuits. These circuits are shown in Table 1, where they are contrasted with conventional CMOS and bipolar circuits.

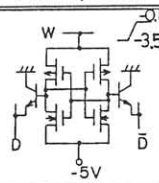
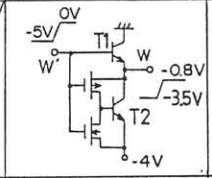
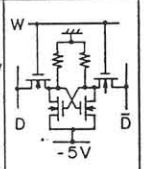
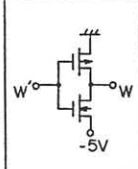
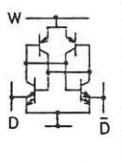
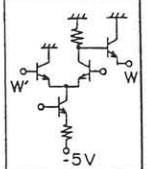
2.1 Memory cell

The BiCMOS memory cell consists of cross coupled pMOS and nMOS FETs combined with bipolar emitter-follower Trs. Therefore, it has two features: negligibly low power dissipation and high speed.

In stand-by, the word line(W) is held at a low level of -3.5V, and the digit lines (D,D) are clamped at a high level of -0.8V . As a result, both bipolar Trs are cut off. Since leakage currents of both the cut-off bipolar Trs and the CMOS flip-flop are extremely low, stand-by power dissipation is kept negligibly low.

During read operation, the word-line level is switched to a high level of -0.8V, and the high-level clamp is removed from the digit lines.

Table 1 Newly proposed BiCMOS circuits, CMOS circuits and Bipolar circuits.

	BiCMOS		CMOS		Bip	
	memory cell	word driver	memory cell	word driver	memory cell	word driver
circuit						
area	~450 μm^2	~3000 μm^2	~300 μm^2	~2000 μm^2	~600 μm^2	~4000 μm^2
power (5V,20MHz)	~1 nW	~3 mW	~1 nW	~3 mW	~10 μW	~10 mW
process device	double level poly-Si gate length : 2μm, t_{ox}: 35nm minimum emitter size : 2x2μm^2, f_T:4GHz		double lebel poly-Si gate length: 2μm, t_{ox}: 35nm		minimum emitter size: 2x2μm^2 f_T : 4GHz	

Then, flip-flop stored information (node voltages) is read out as digit-line voltages of -2V and -4V, according to the stored information. This read operation is performed through the emitter-follower Trs, which allow high current (2mA or more) to flow. Therefore, high speed access is possible, since very fast charging or discharging of the digit-line capacitance is possible.

Another advantage of this memory cell is that read current flows only through the selected cell connected to both the selected word line and the selected digit line. In the case of a CMOS memory cell, read current flows through all the cells connected to the selected word line. Therefore, operating power dissipation in the BiCMOS memory cell array is much lower than that in a CMOS memory cell array.

The write operation is achieved as follows. A low level voltage of -4.5V is applied to one of two digit lines, according to the information. The base voltage of the bipolar Tr connected to that digit line is, therefore, at a low level of -3.5V, causing the flip-flop to invert.

2.2 Word driver

The BiCMOS word driver circuit shown in Table 1 also has low-power and high-speed features. When a low level input is applied, the bipolar Tr, T2, turns on because the pMOS FET turns on, and the bipolar Tr,T1,turns off. Thus,the capacitive load is quickly discharged. After discharging, no steady current flows through T2 because the pMOS FET turns off. When the input increases to a higher level, T1 turns on and quickly charges up the capacitive load. On the other hand, T2 turns off because the nMOS FET turns on with the pMOS FET off. After charging, the output level is high and no steady current flows through T1. In both cases, the two bipolar Trs (T1,T2) always operate in the non-saturated mode. Therefore, high-speed bipolar Tr operation is realized.

3. Results

A 16bit memory test chip fabricated to prove the high performance of these BiCMOS circuits is shown in Fig.1 . It was fabricated using the 2um BiCMOS process described in Table 1. Due to the small capacity of the 16bit memory, additional word-line, C_W, and digit-line, C_D, capacitances are incorporated to evaluate the speeds corresponding to larger capacity RAMs.

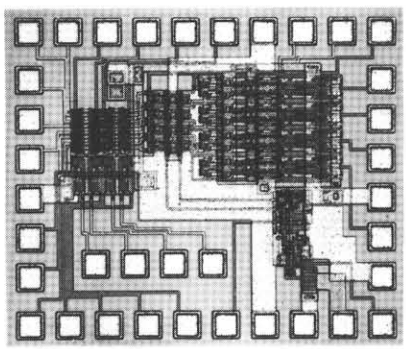


Fig.1 Microphotograph of the BiCMOS memory test chip.

The essential circuits of this memory test chip are shown in Fig.2 . In this figure, read operation is performed by sensing the digit-line voltage differnce using a BiCMOS sense amp. The read current circuit and the write circuit are omitted. The memory cell and the word driver (WD) in Fig.2 are the same as those shown in Table 1. The Data Output signal level is compatible with the ECL logic level (High:-0.9v, Low:-1.7v) .

Simulated waveforms of the main node voltages are shown in Fig.3 . The node marks correspond to those in Fig.2 . The simulated conditions of Fig.3 are word-line capacitance, C_W, of 3pF, digit-line capacitance, C_D, of 5pF and sense-line capacitance, C_S, of 1.2pF. From this figure, it is easy to see that the memory-cell voltage difference between node B_{11} and B_{01} ,or B_{12} and B_{02} does not reduce during the transition period of the word lines (W1,W2). Therefore, the stored data of the memory cell is stable.

Successful write/read operation of the BiCMOS memory test chip is shown in Fig.4 .

Memory cell delay time,td, from a word line to a digit line is shown in Fig.5 . It should be noted that the BiCMOS memory cell offers a td that is about 1/2 to 1/3 that of a conventional CMOS memory cell.

Delay time and power dissipation for the various word driver circuits is shown in Fig.6 . It is cleary shown that the BiCMOS driver provides the highest performance when C_W is larger than 0.3pF . However, CMOS is best for C_W smaller than 0.3pF . This is because intrinsic delay time is dominant in this light-load region. Therefore,CMOS,having the shortest intrinsic delay time, is best.

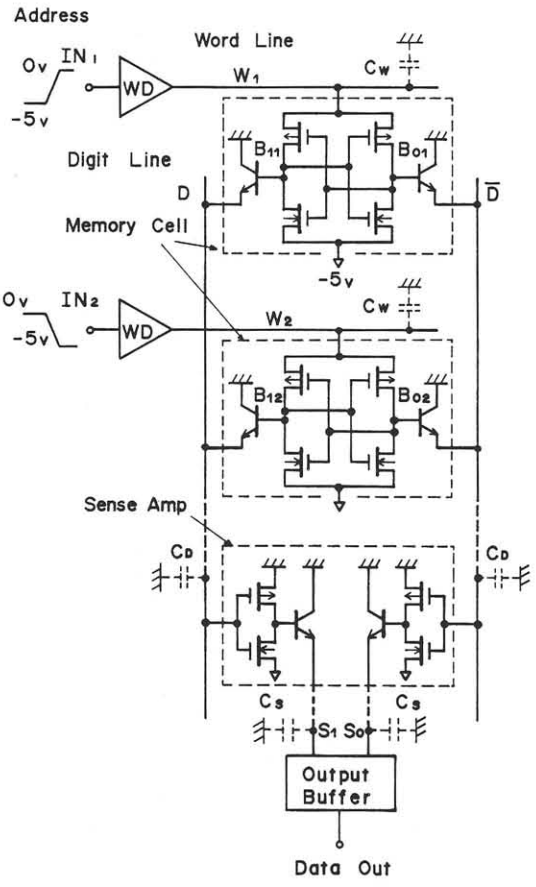


Fig.2 The BiCMOS memory test chip circuit.

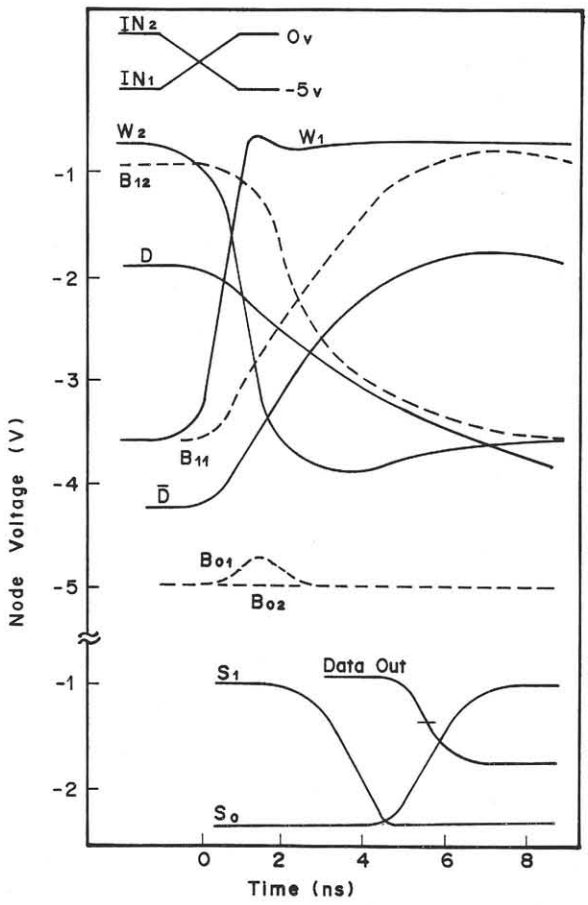


Fig.3 Simulated waveforms of the chip node volatages. C_W=3pf, C_D=5pF, C_S=1.2pF.

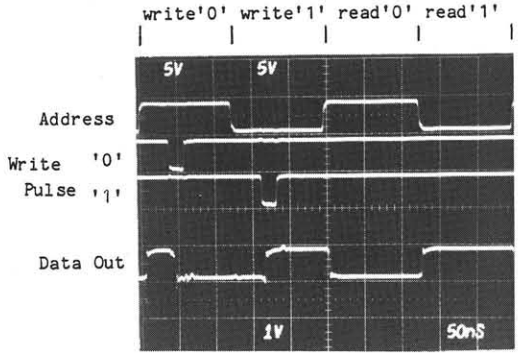


Fig.4 Input/output waveforms of write/read operation.

To further confirm the advantages of BiCMOS circuits, the performance of a fully-decoded BiCMOS static RAM was simulated on the basis of the above results. The simulated results forecast the outstanding features of the newly proposed BiCMOS RAM, i.e. its excellent power-access product of less than half that of conventional CMOS or bipolar RAMs.

4. Conclusions

As the first step to realize low-power, high-speed, high-density static RAMs, a new BiCMOS memory cell and a new BiCMOS driver circuit have been proposed and evaluated by experiment and simulation with the following results.

(1) The BiCMOS memory cell, consisting of cross-coupled pMOS and nMOS FETs with bipolar emitter-follower Trs, provides both low power and high speed.

The BiCMOS driver circuit consists of totem-pole bipolar Trs, and nMOS and pMOS FETs to control those bipolar Trs. This circuit has low power dissipation and very fast switching speed.

(2) As shown by the experiments on the memory test chip, the BiCMOS memory cell operates stably and read operation delay time is less than half that for the CMOS cell. The BiCMOS driver circuit is also shown to provide low power and high speed.

(3) The performance of a fully-decoded BiCMOS static RAM is projected to have a power-access product of less than half that of a conventional CMOS or bipolar RAM.

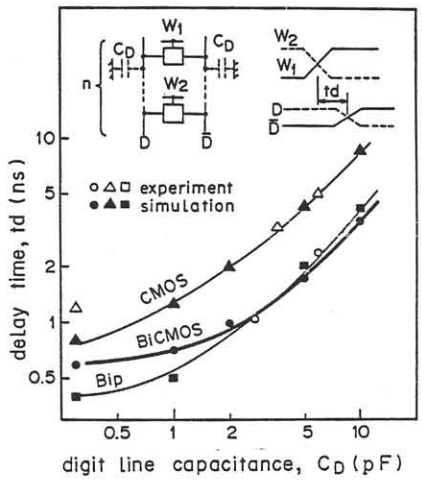


Fig.5 Delay time vs. digit-line capacitance.

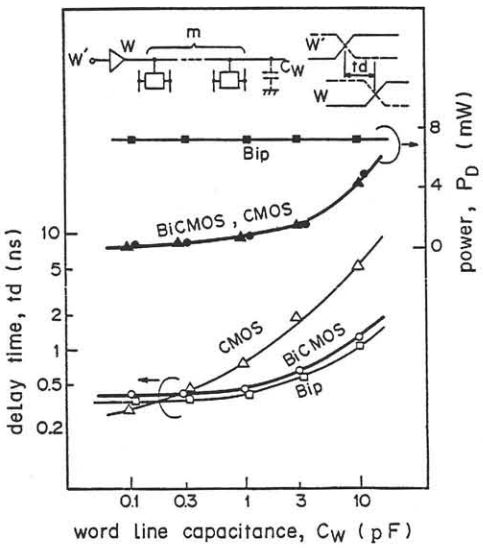


Fig.6 Delay time vs. word-line capacitance.

5. Acknowledgement

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References

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