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Invited

Scaled CMOS and Latch-Up Analysis

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Latch-up phenomenon is analyzed in scaled CMOS, where an epitaxial wafer or trench isolation is introduced. Latch-up susceptibility is markedly increased in an eptaxial wafer CMOS, and trench isolation, in conjunction with an epitaxial wafer, has a potential to realize latch-up free condition. These are well explained by considering the modulation effect of well and substrate resistances and the high injection effect of the bipolar transistors in the parasitic SCR circut. In addition, transient analysis has been established using a charge control model. The model quantitatively explains the latch-up susceptivity depending upon the pulse width of triggering current.

§1. INTRODUCTION

With reduction of device geometry in bulk CMOS LSI's, well and substrate resistances and current gains of parasitic transistors are increased and an SCR type latch-up has emerged as a density limiting problem. Therefore, to keep latch-up susceptibility in scaled CMOS, new structures such as twin-tub[1], epitaxial wafer[2], buried layer[3] or trench isolation[4),5),6] have been proposed and examined. However, the quantitative analysis of the latch-up susceptibilities in the new structures is not sufficient yet.

In this paper, the triggering and holding conditions of parasitic SCR circuits are analyzed considering the resistance modulation effect and the high injection effect of parasitic transistors. And the effect of an epitaxial wafer and trench isolation is discussed. Transient phenomenon of latch-up is also examined and analyzed using a charge control model.

§2. THE METHOD OF LACTH-UP ANALYSIS

A schematic cross section of the n-well CMOS inverter and the top view of the measured pattern are shown in Fig. 1. To the figeure is added circuit consisting of parasitic bipolar transistors and resistances. Main feature size of the pattern is 1.2 um and the spacing of n^+-p^+ is 4.0 um. N-well and p-substrate concentrations are 1×10^{16} and 1.5×10^{15} cm^{-3} respectively and well junction depth is 4.0 um.

If the triggering current is injected to the substrate and exceeds to the value enough to turn on the lateral transistor (I_{trg1} in Fig. 1), the current from V_{DD} starts to flow. With increasing the triggering current, the collector current of lateral transistor exceeds to the value enough to turn on the vertical transistor and lacth-up fires on (I_{trg2}).

The critical triggering currents (I_{trg2}) are expressed as follows in both substrate and well injection cases.

$$I_{trg2}(s) = V_{Fl}/r_s + V_{Fv}/B_l r_w \quad \text{.....(1)}$$

$$I_{trg2}(w) = V_{Fv}/r_w + V_{Fl}/B_v r_s \quad \text{.....(2)}$$

where r_s, r_w, V_{Fl}, V_{Fv}, B_l and B_v are substrate and well resistances, forward voltages and current gains of the parasitic lateral and vertical transistors.

Holding current I_H is also an another figure of merit in CMOS latch-up, and the current is expressed by the equation,

$$I_H = \frac{B_v(B_l+1)(V_{Fl}/r_s)+B_l(B_v+1)(V_{Fv}/r_w)}{B_l B_v - 1} \quad \text{.....(3)}$$

To discuss latch-up free condition, holding

current should be taken in account ($I_H \to \infty$).

The parameters r_s, r_w, B_1, and B_v depend upon current levels. Resistances, r_s and r_w, are modulated by minority carrier injection from the on-state bipolar transistors (resistance modulation effect[7]). Figure 2 shows the substrate resistance depending upon the triggering current injected to the substrate. After turning on of the lateral transistor, the value is decreased to a half of the initial value. With this effect, I_{trg2} is increased by factor two from the value simply expected as shown in Fig. 3.

Figure 4 shows the current gains of the lateral and vertical transistors. In high injection level, excessive minority carriers are injected to the base region and which causes the increase of the minority carrier concentration to keep the charge neutrality condition. Therfore, the current gains decreases gradually with the increase of the collector current. This high injection effect is distinguishable in the parasitic transistors, since their base impurity concentrations are small.

§3. SCALED CMOS STRUCTURE

First of all, we compare the latch-up susceptivity of p-well and n-well CMOS (Table 1). As shown in the table, n-well CMOS is superior to p-well in triggering mode. In p-well CMOS a well triggering current is smaller due to a high well resistance. Since holding current is approximately a summation of the well and substrate critical triggering currents, it is larger in p-well CMOS.

By utilizing an epitaxial layer formed on a high concentration substrate, $I_{trg2}(s)$ is increased by one or two orders of magnitude, owing to the reduction of the substrate resistance. However, in the case of the well injection, the increase of $I_{trg2}(w)$ is not simple. As shown in Fig. 5, in sample B with the relatively high substrate resistance, the lateral transistor turns on immediately after turning on of the vertical transistor due to the high current gain of vertical pnp transistor. The second term of eq.(1) $(V_{F1}/B_v r_s)$ is small. While, in sample A with relatively smaller substrate resistance, the lateral transistor does not turn on easily after turning on of the vertical transistor. Due to the smaller substrate resistance, the higher collector current of the vertical transistor is required to turn on the lateral transistor, where the current gain is decreased to smaller than unit by the high injection effect as shown in Fig. 4, and the second term dominates in eq.(1). As a result, $I_{trg2}(w)$ is sufficiently increased.

Trench isolation is a technology to minimize the n^+-p^+ spacing. Furthermore, combined technology of trench isolation and an epitaxial wafer (Fig. 6) has a potential to realize latch-up free condition in bulk CMOS. To hold latch-up state, a collector current of a vertical transistor must be large enough to bias a substrate resistance and to turn on a lateral transistor. Similar to the case of an epitaxial wafer CMOS, an actual current gain of a vertical transistor is sufficiently decreased due to the high injection effect. And, if a current gain of a lateral transistor is reduced by trench isolation enough to realize that beta product is smaller than unit, latch-up free condition can be realized.

Figure 7 shows the current gain of the lateral pnp transistor in trench isolated p-well CMOS. Though the structure is not optimized yet, the current gain of the lateral transistor is decreased by factor three compared with the conventional structure, and beta product, $B_1 B_v$, is nearly equal to unit. And it is assured that further optimization, such as deeper and wider trench isolation and high substrate concentration, will realize latch-up free condition.

The critical triggering current is rapidly increased, if the input pulse current width is decreased below the base transient time of the parasitic transistor. The analysis using a charge control model has been established and well explains the the measured data (Fig. 8). In the analysis, are utilized measured values of transient times both for lateral and vertical transistors, current gains and parasitic resistances including the high injection effect and the modulation effect.

The reduction of base transient times can not be avoided with decreasing the device feature sizes, such as well depth and n^+-p^+ spacing, therefore scaled CMOS becomes more sensitive to

short pulse current noises. This characteristics is one of the reasons to require new structures in scaled CMOS.

§4. CONCLUSION

The resistance modulation effect and the high injection effect of current gains play important roles to analyze latch-up susceptivity. To use an epitaxial layer enhances not only $I_{trg2}(s)$ but also $I_{trg2}(w)$. The increase of $I_{trg2}(w)$ is explained by the reduction of current gain of a vertical transistor due to the high injection effect.

Trench isolation technology reduces a current gain of a lateral transistor, in conjunction with an epitaxial wafer, and has a potential to realize latch-up free condition in bulk CMOS.

The transient behavior of latch-up is well understood using a charge control model including measured current gains, parasitic resistances and base transient times, and the result requires advanced structures in scaled CMOS.

ACKNOWLEDGEMENT

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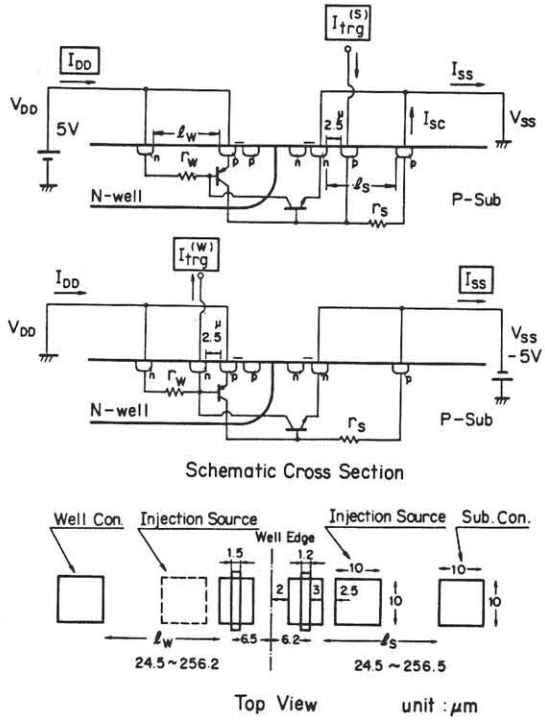

Fig.1 Schematic cross section and top view of a measured n-well CMOS pattern.

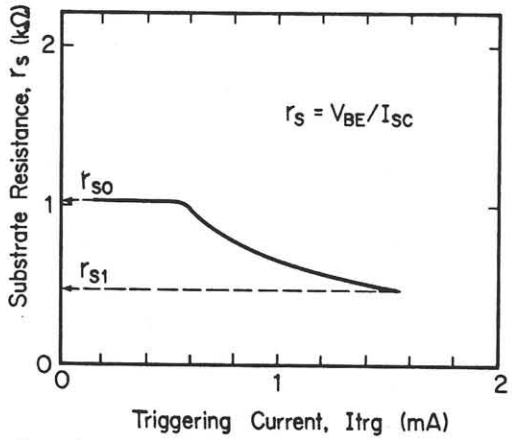

Fig.2 P-substrate resistance dependence on triggering current injected to p-substrate.

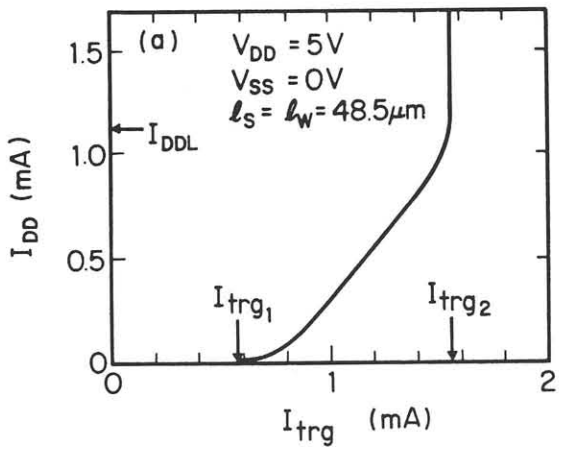

Fig.3 Dependence of the current from V_{DD} supply on triggering current injected to p-substrate.

Table 1 Latch-up susceptibility of p-well and n-well CMOS.

	TRIGGERING CURRENT (mA)			HOLDING CURRENT (mA)
		WELL	SUBSTRATE	
P-WELL $N_{SUB}=1.3\times10^{15}/cm^3$ $N_{WELL}=1\times10^{16}$	I_{TRG1}	0.35	1.7	7.0
	I_{TRG2}	0.73	4.8	
N-WELL $N_{SUB}=1.5\times10^{15}$ $N_{WELL}=1\times10^{16}$	I_{TRG1}	0.8	0.6	2.7
	I_{TRG2}	1.2	1.3	

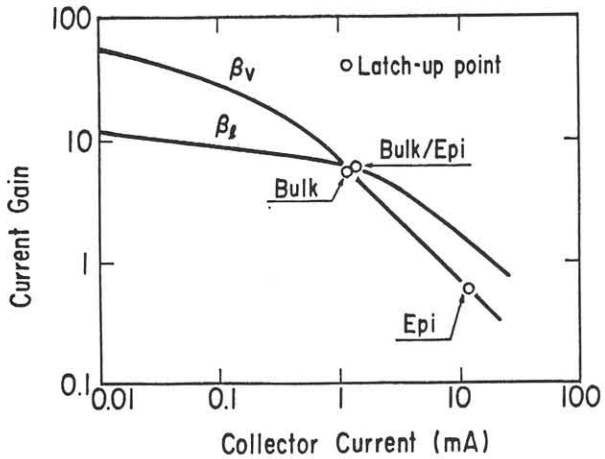

Fig.4 Current gains of the parasitic transistors in n-well CMOS.

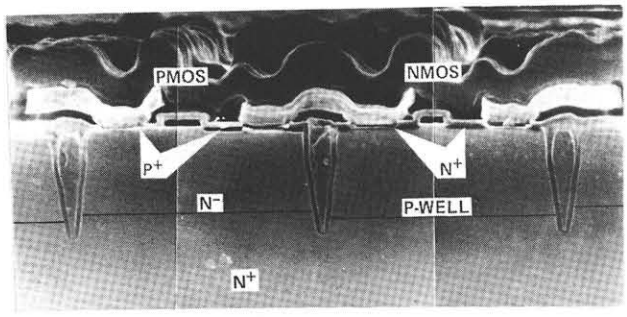

Fig.6 Photomicrograph of p-well CMOS with trench isolation.

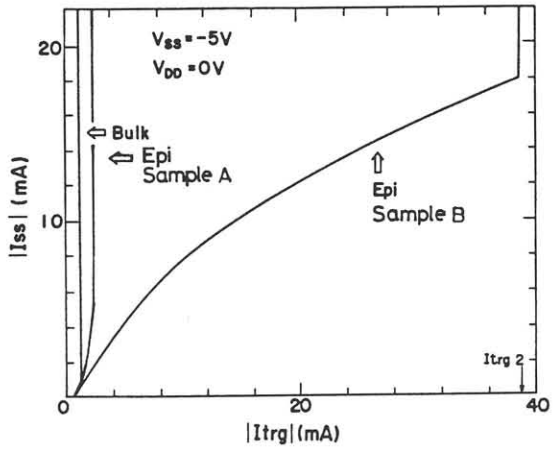

Fig.5 Well injection triggering characteristics of epitaxial wafer n-well CMOS.

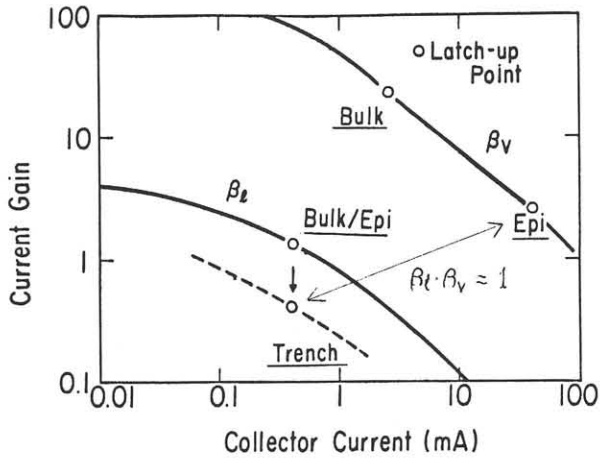

Fig.7 Current gains of the parasitic transistors in p-well CMOS with trench isolation.

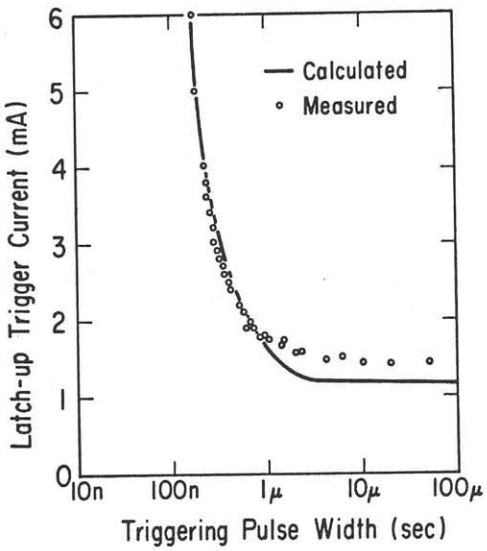

Fig.8 Transient latch-up characteristics.