A CMOS Latch-Up Model Including Non-Linear Effects

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A two-dimensional numerical analysis including carrier recombination determines that the current gain of the parasitic lateral transistor and the substrate parasitic resistors are significantly modulated in latch-up process. These non-linear effects are due to field aided effect and excess minority carrier injection. A simple two-transistor circuit model incorporating these non-linear effects can accurately explain experimental data for transient latch-up behavior.

1. Introduction

One major constraint to scale-down of bulk CMOS is latch-up phenomenon. Latch-up can be triggered by various noises such as displacement current at power-up mode, external current entering I/O signal lines or power-bus lines, and internal noise coming from adjacent circuits. These noises are generally pulsive. Therefore, a study of transient latch-up modeling and analysis is of practical value in preventing or controlling latch-up. Several authors have reported on analysis and modeling of transient latch-up characteristics. However, their models ignore non-linear effects in the parasitic thyristor which could be dominant for latch-up in scaled CMOS LSIs.

This paper presents a simple but accurate model of transient latch-up for external current noise. It incorporates the non-linear effects of current gain, transit time, and base-emitter shunting resistance for parasitic bipolar transistors. The thyristor's non-linear behavior was confirmed through a two-dimensional numerical DC analysis including carrier recombination. Validity of the model was verified through comparison of calculations with experiments for transient latch-up behavior.

Fig.1 Device structure for latch-up analysis

2. Two-dimensional Numerical Analysis

To investigate detailed latch-up mechanism, a 2-D device simulator program TRANAL was utilized. This program self-consistently solves Poisson's equation and current continuity equations for electrons and holes in a 2-D cross section of the semiconductor devices. These equations include S-R-H and Auger carrier recombination models, avalanche model, Shockley-Read mobility model, and Slotboom band-gap narrowing model. Therefore, simulation provided accurate solutions even for latch-up under very high field and excess minority carrier injection.

Device structure for latch-up analysis is shown in Fig.1. Anode to cathode distance and N-well depth measure 12μm and 5μm, respectively. Base
widths of the vertical and lateral transistors are estimated to be 4.6µm and 6µm, respectively. A large analysis area (82µm wide and 280µm deep) is taken to treat the wide spread of excess minority carriers injected into low doped substrate. Impurity profiles of the device structure are shown in Fig.2. The latch-up process can be simulated by applying \( V_{g+} \) or \( V_{g-} \) to the substrate or well contacts in Fig.1. \( V_{g+} \) must be higher than \( V_{PS} \) or \( V_{g-} \) lower than \( V_{DD} \) to fire latch-up. Calculated \( I_n \) vs. \( I_A \) (collector current) characteristics are shown in Fig.3. The solid line was calculated for lateral transistor \( Q_n \) in the substrate triggered (applying \( V_{g+} \)) latch-up operation. It was found that \( I_n \) in the latch-up operation begins to increase from just prior to latch-up onset as compared with current gain in a single operation without the vertical transistor (the dashed line). This was due to the lateral electric field resulting from vertical transistor collector current flow in the base region. This suggests that the base transit time could also be affected and reduced by the field aided effect.

The collector current dependencies of substrate parasitic resistance \( R_{PS} \) and well parasitic resistance \( R_{NW} \) in the latch-up process are shown in Fig.4. Significant conductivity modulation is observed in \( R_{PS} \), even before latch-up for the substrate triggering mode because excess electron carriers are injected into the low doped substrate base region and spread widely. On the other hand, \( R_{NW} \) was almost unchanged for the well triggering mode because the well-substrate junction suppressed minority carrier spread. After latch-up, both \( R_{PS} \) and \( R_{NW} \) are highly modulated. Measured collector current dependencies of \( R_{PS} \) and \( R_{NW} \) (dashed lines in Fig.4) are similar to calculated results. Magnitude difference between experiments and calculations was explainable on a three-dimensionally spreading current which was not treated in the calculation.

3. Transient Latch-up Model

To investigate how the foregoing non-linear effects change transient latch-up characteristics, these effects in the conventional two-transistor model were introduced and the calculations were compared with the experiments. The equivalent
circuit model for the substrate triggering is
shown in Fig.5. The Gummel-Poon model \(^7\) is used
for bipolar transistors. The non-linear expression
functions are derived from the consideration of
two-dimensional analysis:

1) current gain \( \beta \) and total forward transit time
\( \tau_{\text{FNO}} \) for the lateral transistor:
\[
\beta = \frac{\xi \cdot \beta_{\text{NO}}}{1 + (1/\beta_{\text{PP}})^{1/2}}
\]
\[
\tau_{\text{FNO}} = \frac{\tau_{\text{FNO}0}}{1 + (1/\beta_{\text{PP}})^{1/2}}
\]
where \( \beta_{\text{PP}} \) is the vertical transistor collector
current, \( \beta_{\text{NO}} \) and \( \tau_{\text{FNO}0} \) are current
gain and forward transit time of the lateral
transistor in the single operation and include
the high injection effect (as a parameter of
Knee current \( I_{\text{K}} \)).

2) conductivity modulation resistors:
\[
R = \frac{R_0}{1 + K \cdot I_E}
\]
where \( I_E \) is the emitter current, \( K \) is the
modulation coefficient, and \( R_0 \) is the unmodu-
lated bulk resistance. All resistor values
except \( R_{\text{EP}}, R_{\text{EN}}, R_{\text{PS}}, \) and \( R_{\text{MD}} \) were regarded
as being modulated because they are located in
the base regions.

Pulse width dependencies of the latch-up trigger
current calculated using this model are shown in
Fig.6 (for a device with 6 \( \mu \)m base width lateral
transistor) and Fig.7 (for a device with 2 \( \mu \)m base
width). Calculations taking the whole non-linear
effect into consideration were in good agreement
with experiments. However, calculations excluding

![Fig.5 Equivalent circuit model of transient latch-up for the substrate triggering](image)

![Fig.6 Pulse width dependencies of latch-up triggering current with lateral transistor base width 6 \( \mu \)m](image)

![Fig.7 Pulse width dependencies of latch-up triggering current with lateral transistor base width 2 \( \mu \)m](image)

![Fig.8 Calculated and measured waveforms for latch-up turn-on current](image)
conductivity modulation were much different from experiments. In addition, calculation ignoring conductivity modulation could not fully explain the experiment even in the DC threshold trigger current level.

The corresponding device structure and profile are similar to the device in Fig.1 and 2. Element values of the equivalent circuit used for calculation are listed in Table I. These values are determined as follows.

1) $\beta_{no}$, $\beta_{po}$, $T_{Fno}$, $T_{Fpo}$, $T_{E}$, $R_{EN}$, $R_{PS}$, and $R_{NW}$ (including $R_{o}$ and $K$) are measured from the parasitic transistors using the well-known measurement method.6)

2) $R_{CP}$, $R_{BN}$, $R_{CN}$ and $R_{BP}$ are estimated from the device structure and profile. They become negligibly small at the latch-up onset due to conductivity modulation.

3) $C_{JN}$, $C_{JP}$, $C_{JC}$ are estimated from the impurity profile.

4) $A_{1}$, $B_{1}$, $A_{2}$ and $B_{2}$ in eq. (1) and (2) were determined from fitting of calculated and measured waveforms for latch-up turn-on current as shown in Fig.8 because they could not be measured from the actual devices.

| Table I |
|-------------------|-------------------|
| $R_{no}$ : $\beta_{no}$ = 2.0 | $I_{Kn}$ = 5.45 mA |
| $R_{po}$ : $\beta_{po}$ = 10 | $I_{Kp}$ = 10 mA |
| $I_{SN}$ = 1.5x10^{-15} A | $I_{SP}$ = 2x10^{-17} A |
| $R_{EN}$ = 25 $\Omega$ | $R_{EP}$ = 30 $\Omega$ |
| $R_{PS0}$ = 300 $\Omega$ | $R_{NWO}$ = 200 $\Omega$ |
| $R_{PS}$ = 840 $\Omega$ | $R_{NW}$ = 270 $\Omega$ K=1000 |
| $R_{CP}$= $R_{BN}$ = 300 $\Omega$ | $R_{CN}$= $R_{BP}$ = 100 $\Omega$ |
| $C_{JN}$ = 0.1pF | $C_{JP}$ = 0.1pF |
| $C_{JC}$ = 0.4pF |

$T_{Fno}$, $T_{Fpo}$ : $T_{Fno}$ = 50nsec $T_{Fpo}$ = 5.0nsec

$A_{1}$ = 305 $B_{1}$ = 0.44
$A_{2}$ = 11.2 $B_{2}$ = 0.25

$I_{Kn}$, $I_{Kp}$ : Knee current at high injection mode

4. Conclusion

A two-transistor model incorporating non-linear effects such as the field aided effect and the conductivity modulation effect can accurately explain experimental data for transient latch-up behavior. These non-linear effects were determined by a two-dimensional device simulator including carrier recombination. This model required fitting parameters only for the field aided effect on current gain and transit time of the parasitic lateral transistor. Other parameters were determined through measurement of parasitic elements. This simple circuit model should prove indispensable for designing latch-up immunity in scaled CMOS LSIs, when the magnitude element constituting the thyristor can be estimated incorporating their three-dimensional structure effect.

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References