Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 245-248

Monolithic 150V Push-Pull Driver with High-Speed Logic

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A high-voltage Semi-Well Isolation LSI technology that can produce high-voltage, up to 180 V, current sink and source circuits as well as compact high-speed logic circuits with 2-3 ns gate delay, has been developed. To achieve push-pull operation, high-voltage totem-pole type circuits are formed in the thick epitaxial layer, while the isolation regions and logic circuit are formed in the thin portion for compactness. Complementary Schottky Transistor Logic is successfully integrated to meet the high-speed requirement with a modification of epitaxial layer resistivity. As a result, minimum propagation delay time of 2.5 ns/gate was attained. An 8-outputs IC including a shift register and latches was operated with 7 MHz clock and a 150 V push-pull output swing.

1. INTRODUCTION

High-voltage IC which has the capability of both current sink and current source with high-speed compact logic on the same chip, has long been required for display drivers such as a plasma, an EL, or a dot matrix VFD panel. However, most of the high-voltage ICs so far reported have only high-voltage transistor arrays of open-drain MOSFETs as drive circuits [1],[2],[3].

In this paper, a new monolithic IC technology, which is applicable to the realization of driver LSI with push-pull outputs and a high-speed logic that can operate at 7MHz clock frequency, is reported.

2. DEVICE TECHNOLOGY

Device structure

In order to maintain a high-voltage operation, it is well known that devices must be formed on a thick and high resistive epitaxial layer. A thick epitaxial layer requires a deeply diffused isolation layer. Therefore, large chip size due to increased occupied area for isolation raises IC cost. In addition, small signal transistors formed in a thick epitaxial layer have very poor electrical characteristics because of the increase of series collector resistance. This decreases the frequency response of a logic circuit considerably.

The recently developed IC structure " Semi-Well Isolation (SWI) [4] ", which eliminates the above problems, was introduced. A cross-sectional view of SWI structure is shown in Fig.1(a). The special feature of this structure is that it has an epitaxial layer of two different thicknesses. The isolation diffusion is made only in the thin portion of the layer. Therefore, thick epitaxial layer can be employed easily without any troublesome deep isolation diffusion process. Also, since low-voltage devices are formed in the thin epitaxial layer, their electrical characteristics are kept as good as conventional devices.

For a flat panel display driver, high-voltage outputs are required to have the capability of both current sink and current source. In addition, logic circuits are required to have high-speed operation. To meet these requirements, high-voltage totem-pole output circuits are formed in the thick epitaxial portion by using bipolar transistors, and high-speed logic circuits are formed in the thin epitaxial portion.

Bipolar high-speed logic

A Complementary Schottky Transistor Logic (CSTL), which has four times greater

packing density than a conventional STTL and has the same high-speed, was used to satisfy the high-speed requirements of the logic circuitry [5]. A basic CSTL circuit is shown in Fig.1(b). Logic speed of CSTL depends on the resistivity of the epitaxial layer. It has been reported that high resistive epitaxial layer makes logic speed of CSTL lower than that of a low resistive one [5]. This is because, a Schottky Barrier Diode (SBD) does not clamp the base-collector voltage because of influence by the large series resistance.

However, the resistivity of epitaxial layer must be high in order to obtain high-voltage devices on the same chip.

Thus, the thin epitaxial portion must necessarily have lower resistivity than the thick portion, in order to realize high-speed operation. N-wells were introduced in the thin epitaxial portion for that reason. N-wells must have a suitable surface concentration that is possible to form the SBD, and enough depth to reach the n^+ buried layer for reduction of series resistance.

3. EXPERIMENTAL RESULTS

High-voltage devices

High-voltage devices are designed to have a minimum breakdown voltage of 150 V. Therefore the resistivity and thickness of the epitaxial layer are more than 15 ohm-cm and more than 30 um, respectively. To prevent the degradation of p-n junction breakdown voltage due to metal electrodes, ion-implanted layers are used. These are an n-type ion-implanted layer around n^+ diffused layer and a p-type ion-implanted layer around p-diffused layer. These reduce the electric field intensity. Current-voltage characteristics for the fabricated high-voltage devices are shown in Fig.2. Breakdown voltage (BVceo) of 180 V was obtained.

CSTL circuit

CSTL circuit is formed in n-wells diffused in the thin epitaxial portion (thickness about 10 um), in order to reduce the series resistance of SBD. The measured value of an n-well sheet resistance is 610 ohm/square and surface concentration is about 3×10^{16} cm^{-3}. The improvement of series resistance by n-well without increasing SBD's area is shown in Fig.3. The relation between propagation delay time and injector current of a CSTL device measured using a 5-gate CSTL ring oscillator is shown in Fig.4. It shows that npn transistor clamped by SBD with n-well is two times higher speed than that of without n-well. The minimum propagation delay time of 2.5 ns/gate was observed. Using a counter that is composed of a 6-NOR type D-FF, maximum toggle frequency was measured (Fig.5). In spite of high-voltage devices being on the same chip, the highest toggle frequency of 80 MHz was obtained. We made sure that there was no problem of breakdown voltage when using n-well, because of having above 7V of BVceo.

4. CIRCUIT PERFORMANCE

To demonstrate capabilities of this process, a 150 V display driver was fabricated. This driver employs high-voltage bipolar transistors to implement push-pull, totem-pole outputs that sink or source 5mA current at 150V. A photomicrograph of the IC is shown in Fig.6. The chip size is 3.5 mm x 3.5 mm. This IC contains an on-chip 8 bit shift register with a serial input and serial/parallel outputs. The input-output waveforms of the IC are shown in Fig.7. Its totem-pole, push-pull outputs handle supplies as high as 150 V. It is possible for a shift register to operate at 7 MHz clock. Typical characteristics of transistors using in this IC are shown in Table 1.

5. CONCLUSION

A high-voltage LSI technology which can realize driver LSIs including both current sink and current source capabilities and compact high-speed logic, has been developed. This technology was achieved by a combination of high-voltage devices and CSTL circuits in the SWI structure, with two epitaxial thicknesses, based on a p-n junction isolation technique.

ACKNOWLEDGMENTS

The authors wish to thank K.Hoya, I.Shimizu and Y.Nagai of Takasaki Works for their valuable discussions.

REFERENCES

(1) K.Fujii, Y.Torimaru, K.Nakagawa,T.Fujimoto and Y.Aoki, ISSCC 81 pp.46-47

(2) Basil Weir, SID 82 DIGEST pp.268-269

(3) H.Wakawumi, T.Suzuki, M.Saito and H.Sakuma, IEDM 83 pp416-419

(4) I.Imaizumi, M.Kimura, M.Yoshimura and T.Yamaguchi, J.Appl. Phys. Sup.20-1 pp.111-114, 1981

(5) K.Kaneko, Y.Okada, T.Okabe, S.Ogura and S.Kudoh, Trans. IECE Japan (C), J65-4,215-221,1982

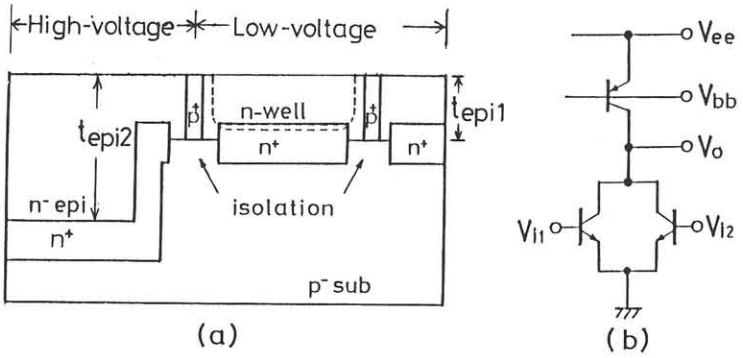

Fig.1 (a) Cross sectional view of SWI structure and (b) a basic CSTL circuit.

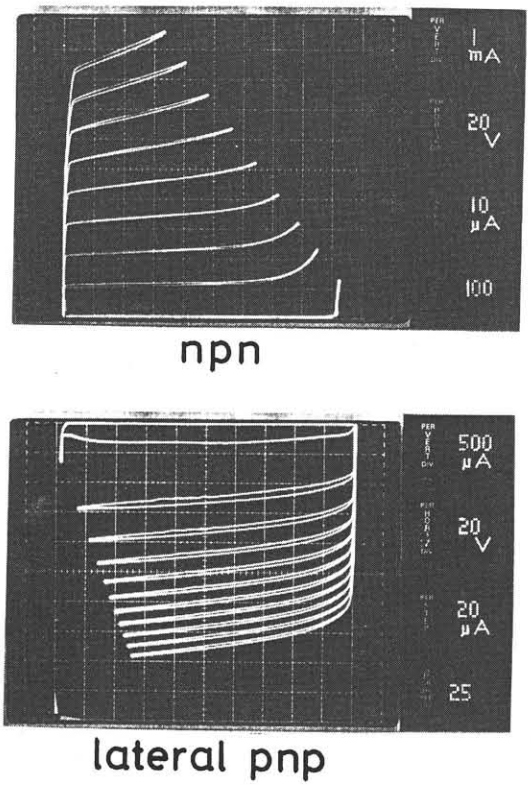

Fig.2 Current-voltage characteristics of high-voltage transistors fabricated in the thick epitaxial portion of SWI structure.

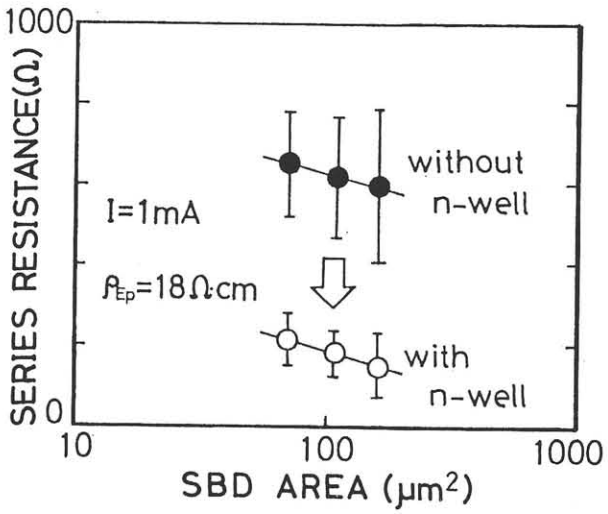

Fig.3 The improvement of series resistance of SBD by n-well.

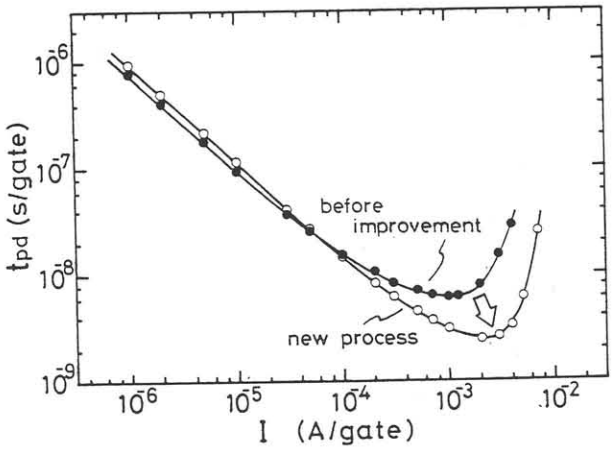

Fig. 4 Propagation delay time of CSTL gates versus injector current.

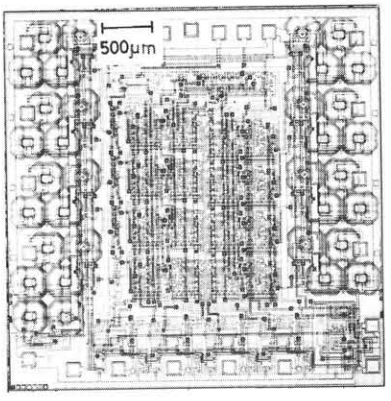

Fig. 6 High-voltage IC with push-pull output stages and CSTL logic circuits.

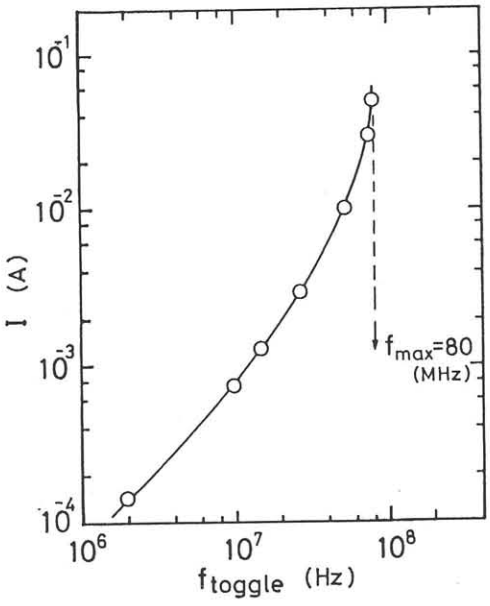

Fig. 5 Toggle frequency versus supplied current as measured on a D-type flip-flop CSTL

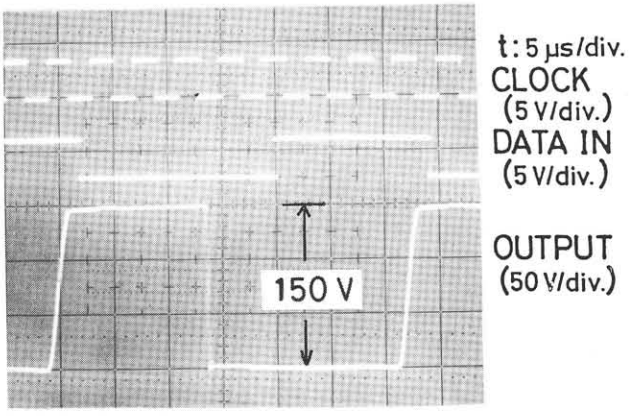

Fig. 7 Input-output waveforms for 150 V operation.

Table 1. Typical characteristics of transistors used in a 150 V IC

	High-Voltage TRS		Low-Voltage TRS		
	npn	pnp	npn		pnp
			with n-well	without n-well	
hFE	97	70	98	78	6.4
BVceo (V)	180	190	9.5	10.8	35
BVcbo (V)	180	190	34.5	36.5	35
BVsub (V)	190	195	92	158	160