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Soft-Error Generation Due to Heavy-Ion Tracks in Bipolar Integrated Circuits

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Soft-error generation due to heavy-ion tracks in integrated circuits (ICs) has become an important phenomenon in the pursuit of high-density LSI and VLSI technology. Bit-errors can be caused by ionization from a single heavy ion (e.g., cosmic-ray particle or alpha particle from radioactive decay) depositing charge in a junction. As the devices (transistors, diodes) contained in future IC chips become increasingly smaller, they will become more susceptible to bit-flips in latch circuits (such as RAM cells) owing to the decrease in the amount of charge required to cause single-event upset (SEU). In this paper the results obtained from the modeling of the critical charge required for SEU in bipolar RAMs are presented.

§1. Introduction

Both bipolar and MOS integrated circuits (ICs) have been empirically demonstrated to be susceptible to single-particle soft-error generation, commonly referred to as single-event upset, or SEU,[1] which is manifested by a bit-flip in a latch-circuit construction (e.g., flip-flop, RAM cell). This phenomenon is caused by the collection of charge (electron-hole pairs) produced by an energetic ionizing particle (heavy-ion track) transversing an active device (transistor, diode) within an IC. Future VLSI chips may contain devices sufficiently small to permit SEU by direct proton charge ionization (or even lighter charged particles, e.g., muons) as well as by heavy ions. The charge is collected at specific junction nodes within the device via both drift and diffusion. Space-charge effects necessitate the use of numerical computation methods for the calculation of charge collection. In this paper the intrinsic characteristics of SEU in bipolar (static) RAMs are demonstrated through results obtained from the modeling of this effect using computer circuit-simulation techniques. In this analysis, the collected charge required to upset a bipolar RAM is examined independently of the charge collection process (i.e., collected charge is treated as an independent parameter).

§2. Bipolar Transistor Macromodel

Bipolar transistor structures to be analyzed for SEU are modeled using an interactive version of SPICE.[2] The device models and subcircuits available in the software are used to construct a macromodel for an integrated bipolar transistor. Time-dependent current generators are placed inside the transistor macromodel to simulate charge collection from an ion track. The structure of an NPN transistor and its corresponding macromodel containing ion-produced current generators and charge-collection nodes are shown in Figures 1 and 2.

The transistor cross section diagram shown in Figure 1 has superimposed on it specific ion tracks which deposit charge at the various junction nodes within the device, corresponding to the particular junction(s) which it intersects. For example, the collected charge from the track which intersects the emitter-base-collector of the kernel NPN transistor is represented by the current generators I_E plus I_C (or I_{B1}) and charge Q_{B1}. The charge Q_{B1} is deposited at the base of the kernel transistor, as depicted in Figure 2. Current generators I_E and I_C derive from the charge collected at the emitter-base and collector-base N-P junctions, respectively. The resistance R_{BE} (emitter-crowding resistance)

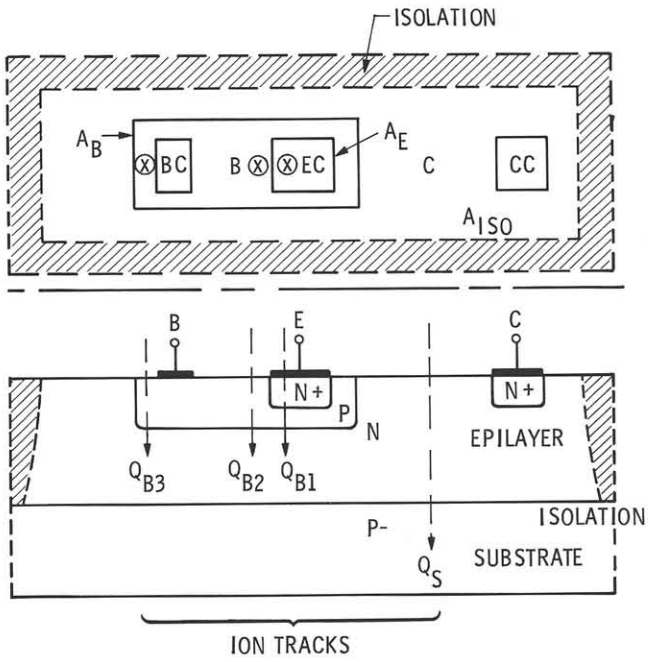

Figure 1. Cross section and plan views of integrated NPN bipolar transistor. B, E, C denote base, emitter, collector; BC, EC, CC denote contacts for base, emitter, collector; A_E is the projected area of the emitter-base junction, A_B is the projected area of the base-collector junction, and A_{ISO} is the total area inside the isolation region (epilayer-substrate junction).

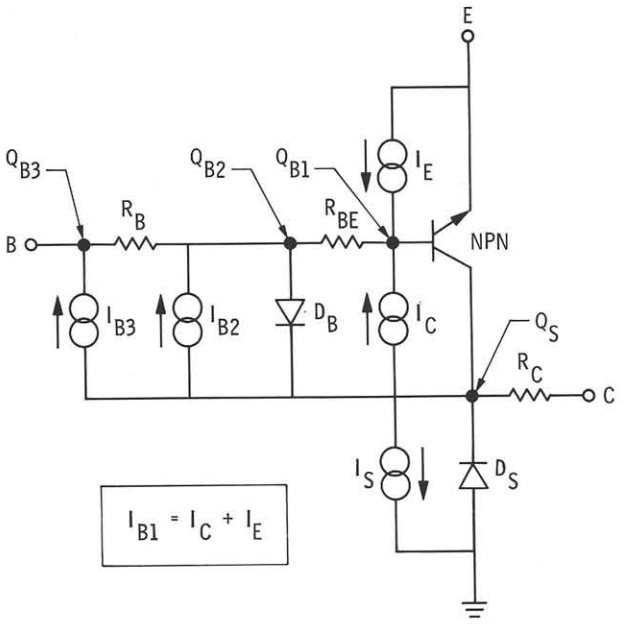

Figure 2. Circuit model for integrated bipolar transistor. B, E, C denote base, emitter, collector.

represents an impedance to current flow into the base region of the kernel transistor from the outer volume of the P-type base diffusion just outside the perimeter of the N+ emitter diffusion. The diode, D_B, represents the P-N junction formed by the intersection of the base diffusion with the epilayer, excluding that portion directly under the emitter diffusion. The resistance, R_B, corresponds to the spreading resistance inside the base diffusion between the perimeter of the emitter diffusion and the base-contact terminal of the device. An ion track which intersects the base-epilayer junction adjacent to the emitter region is represented by the current generator I_{B2} and the integrated charge Q_{B2}. Similarly, an ion track intersecting the base-epilayer junction at the perimeter of the base diffusion is characterized by I_{B3} and Q_{B3}. Finally, the epilayer-substrate N-P junction is simulated by the diode D_S, the current generator I_S, and charge Q_S. The node at which Q_S is deposited is separated from the collector-contact terminal by the spreading resistance, R_C, in the epilayer.

§3. Computer Simulation of SEU in a Bipolar RAM

A circuit diagram which contains the salient features required for SEU simulation of a bipolar RAM cell is shown in Figure 3. The transistors Q_1 and Q_2 are modeled by the subcircuit in Figure 2. Rectangular time-dependent current pulses of width τ and amplitude I_o (simulating a collected charge of τI_o) were used for the current generators in Figure 2. The exact shape (e.g., rectangular vs. double-exponential) of the current pulses used for SEU simulation had virtually no effect, given that the integrated charge and pulse width were of the same magnitude for the different pulse shapes. SEU occurs in the bipolar RAM only when ion tracks pass through the off transistor (i.e., only in Q_1 when V1 is high for a bit of "1," Figure 3).

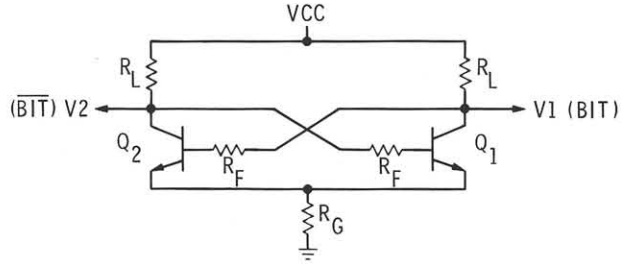

Figure 3. RAM-cell circuit.

Each of the four ion tracks illustrated in Figure 1 exhibits a unique critical-charge value in the SPICE simulations. Furthermore, the geometrical cross section for each type of event can be construed from Figure 1 (the empirical definition of SEU cross section is the number of errors per bit divided by the ionizing-particle fluence); e.g., Q_{B1} events would have a cross section equal to the projected area A_E in the plan view of the emitter diffusion. For ion tracks adjacent to the emitter diffusion, the simulations show that the critical charge Q'_{B2} is higher in value than Q'_{B1}. This result derives from the presence of the emitter-crowding resistance, R_{BE}, in the transistor model. For ion tracks which pass through the perimeter of the base diffusion, an even larger critical charge Q'_{B3} is obtained from the simulations owing to the resistance R_B in the transistor model. The latter class of events has a cross section equal to the projected area A_B of the base diffusion. The cross section for ion tracks passing between Q_{B2} and Q_{B3} is approximated by a linear interpolation between A_E and A_B. Finally, ion tracks which intersect only the epilayer-substrate junction exhibit yet a larger critical charge Q'_S. This type of event has a cross section equal to the area A_{ISO} circumscribed by the isolation region. Figure 4 shows the cross section for SEU in a bipolar RAM cell as a function of collected charge as described above.

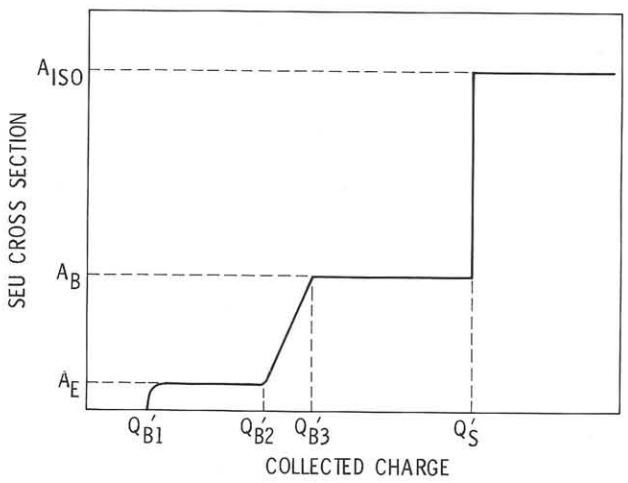

Figure 4. Plot of SEU cross section vs. collected charge.

§4. Conclusions

The overall results of the simulations for SEU in bipolar RAMs discussed in the foregoing paragraphs may be applied to most design and processing schemes in both present and future technology. As the magnitude of the device dimensions decreases, the critical-charge values decrease in proportion to the values of the cross sections. The analysis given here may be expanded to encompass more complex RAM-cell structures plus other latch circuits and varied process parameters (e.g., diffusion doping profiles) by simple modification of the circuits and device models used in the SEU simulations. Some possible modifications which may easily be implemented are: (1) Schottky-diode clamped transistors; (2) diffused or ion-implanted resistors which may contain charge-collecting junctions; (3) buried-layer structures (N+ diffusion in the P-type substrate); and (4) other devices within the isolated RAM cell (diodes, transistors) which may be included to implement read/write operations or special biasing of the memory transistors.

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