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Circuit Simulation with Two-Dimensional MOST Models

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A new numerical MOST model is presented which has been implemented in a modular mixed-level circuit simulator. This concept allows to predict circuit behaviour based on technological input data. Sensitivity analysis can simply be done by varying doping profile or geometry. The efficiency and flexibility of the new MOST model is shown by simulations of a CMOS RAM cell.

1. Introduction

For accurate simulation of integrated circuits accurate device models and model parameters are mandatory. With decreasing device geometry the influence of parasitics increases and analytical models fail, especially if predictive capabilities are needed. Several attempts have been made to overcome this problem. E.g. in /1/ the device equations are solved in a quite simple circuit environment. A different approach but only for the bipolar case was presented in /2,3/, where a numerical device simulator and a general purpose circuit simulator are merged in a mixed-level simulator enabling the consistent solution of the coupled system of circuit equations and partial differential equations describing the devices. A new approach following this concept for the MOS case is presented.

2. Description of the model

The key to this approach is a highly efficient numerical MOST model. For this model Poisson's equation in two dimensions and the continuity equation of one carrier in one dimension are solved simultaneously. Comparison with the results of the exact two-dimensional simulator GALENE shows only small deviations in drain current even for short channel devices /4/. An improved discretization formula for Poisson's equation allows coarser grids than the conventional approach resulting in considerable savings of memory and CPU time. Important physical effects like velocity saturation and mobility reduction due to the perpendicular electrical field are taken into account. Because the fundamental differential equations are solved, this model includes subthreshold, punch-through and short channel effects on a sound physical basis in contrast to analytical models.

3. Implementation in MEDUSA

This new model has been implemented in the user oriented modular circuit simulator MEDUSA as a special k-module /5/. Backward differentiation formulae /6/ up to order six with automatic control of step size and order are used to discretize the time derivatives meeting stability and efficiency requirements. The Newton-Raphson method is applied to solve the resulting nonlinear system of device and circuit equations. The Jacobian is of bordered block diagonal form. Block relaxation method first proposed in /2/ is used to solve this large system efficiently reducing the required amount of storage drastically.

The MOST model needs only technological input parameters like doping and geometry data which can be obtained e.g. from a process simulation. This allows the designer to predict the performance of MOS transistors embedded in a realistic circuit

environment providing realistic bias and input waveforms or to familiarize oneself with the sensitivities of the circuit performance with respect to technological parameters. Optimization can simply be done by varying doping profiles and geometry.

4. Examples

A static CMOS RAM cell shown in Fig. 1 is used to exemplify how to take advantage of the new simulation tool. All MOS transistors are described by the new numerical model. The drain-bulk diodes as shown in the circuit diagram are modelled by a one-dimensional numerical bipolar model /3/. The circuit is described in conventional manner for the input of the general purpose network simulator MEDUSA.

The influence of channel length on device and circuit performance is studied by means of several steady state and transient simulations as follows. The doping profiles result from SUPREM simulations for a standard CMOS process. For the simulations all MOSTs are discretized with 368 grid points and the diodes with about 50 grid points. The simulation of 30 ns of a write cycle required 609 time steps and 1612 Newton iterations where in each iteration more than 2800 linear equations had to be solved resulting in a total CPU time of approximately 6 1/2 hours on a DATA GENERAL ECLIPSE MV/10000 minicomputer.

Write and read cycles for 1.4, 1.6, 1.8, and 2.0 micron gate length (mask dimensions) have been simulated. In addition for these four cases the stand by power consumption has been determined. To give insight into the circuit performance of the 1.4 micron gate cell Fig. 2 to 4 show simulated waveforms of node voltages and currents for the write cycle and Fig. 5 to 6 for the read cycle, respectively. In the read case the transmission gate T1 stays in "off" state due to high V_{bs} voltage so that the voltage of node 2 is not affected. The high quiescent current I4 is remarkably large. To find out the reason for this behaviour one can look into the operating devices under their circuit constraints. The mixed level simulator gives not only access to the external node voltages of the devices embedded in the circuit but also to their internal distributions. In Fig. 7 the high carrier density below the channel indicates that this device is punching. Though a reduction of gate length improves access times somewhat (Fig. 8) the worsening effect on stand by power dominates overall circuit performance. A better compromise can be found at a somewhat larger channel length by reducing the junction depth of the channel implantation. Comparing the corresponding results (Fig. 8) for both profiles proves this idea.

5. Conclusion

A numerical MOST model has been presented allowing its implementation in the mixed mode simulator MEDUSA. This approach combines characteristics of a network analysis program and of a highly efficient MOS device simulator. The utility and flexibility of the new tool has been illustrated by simulations of a CMOS RAM cell.

<u>References</u>

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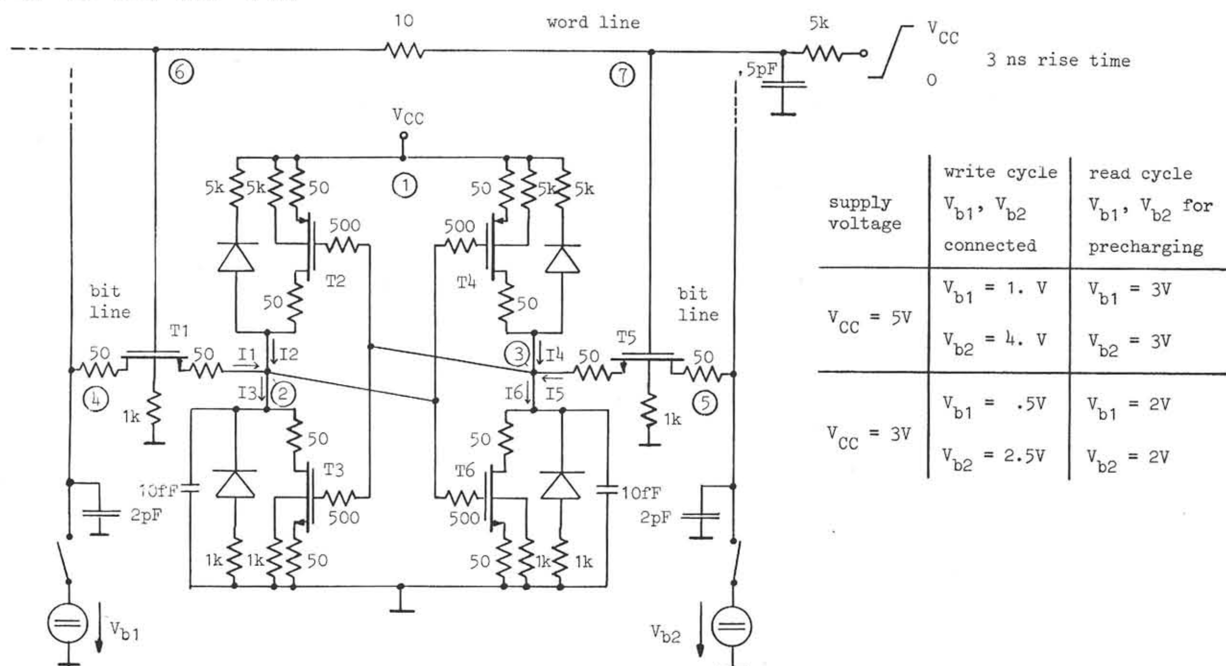

supply voltage	write cycle V_{b1}, V_{b2} connected	read cycle V_{b1}, V_{b2} for precharging
V_{CC} = 5V	V_{b1} = 1. V V_{b2} = 4. V	V_{b1} = 3V V_{b2} = 3V
V_{CC} = 3V	V_{b1} = .5V V_{b2} = 2.5V	V_{b1} = 2V V_{b2} = 2V

Fig. 1 Simulated CMOS RAM cell and applied voltages

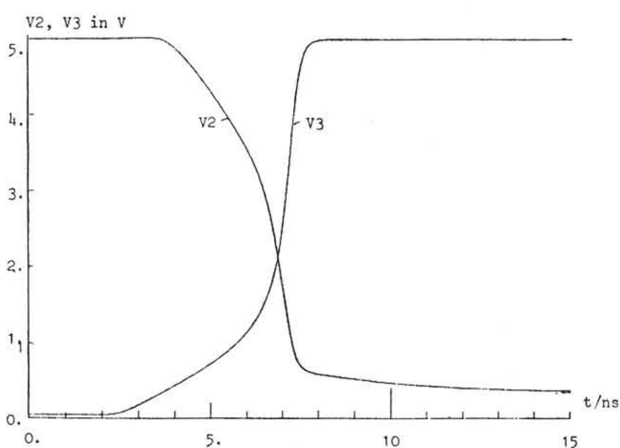

Fig. 2 Node voltages V2(t), V3(t) for write cycle, 1.4 μ gate length, V_{cc} = 5V

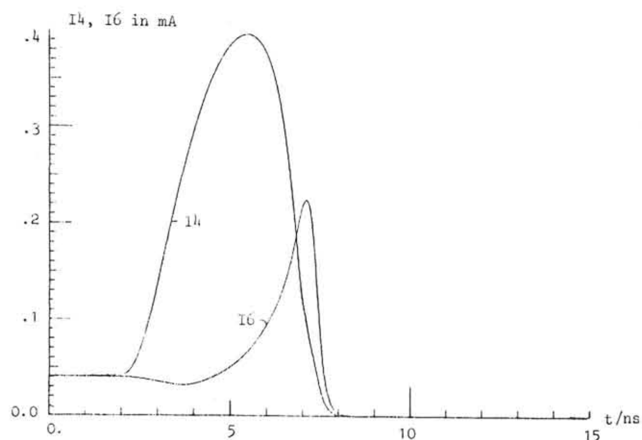

Fig. 4 Currents I4(t), I6(t) for write cycyle as fig. 2

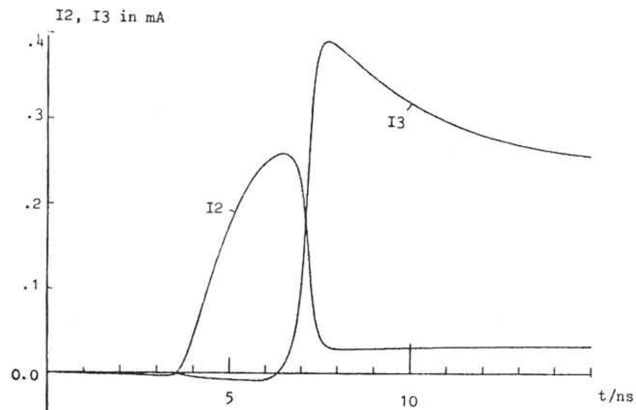

Fig. 3 Currents I2(t), I3(t) for write cycle as fig. 2

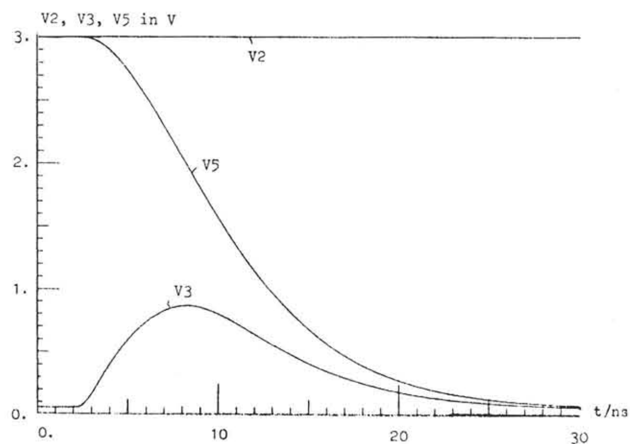

Fig. 5 Node voltages V2(t), V3(t), V5(t) for read cycle, 1.4 μ gate length, V_{CC} = 5V

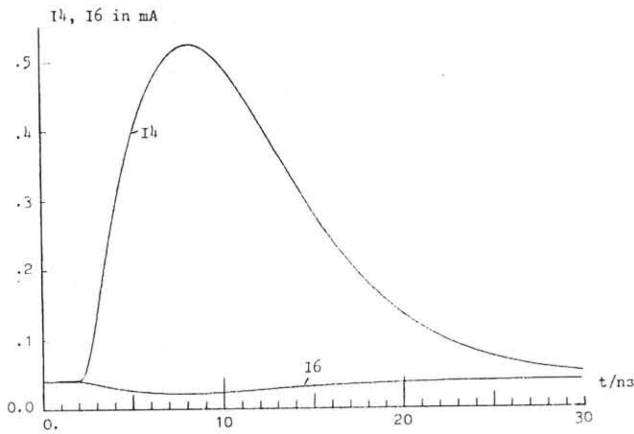

Fig. 6 Currents I4(t), I6(t) for read cycle as fig. 5

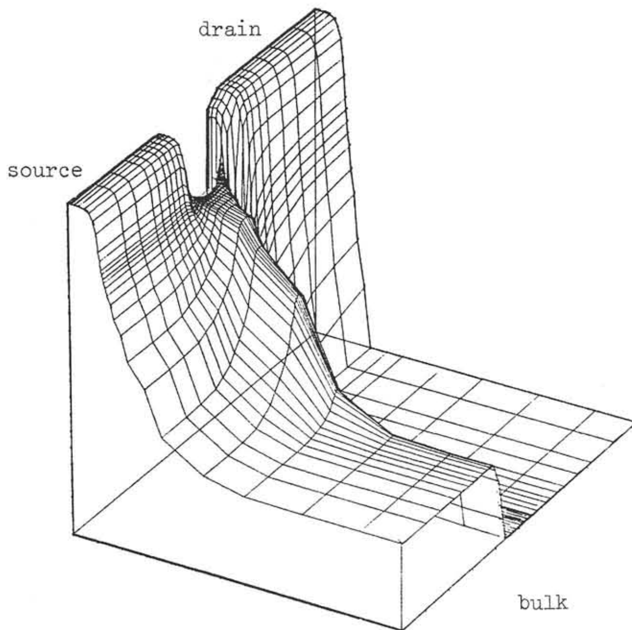

Fig. 7 Two dimensional hole distribution (log. scale) for 1.4 μ gate length p-channel transistor T4 before switching ("off" state).

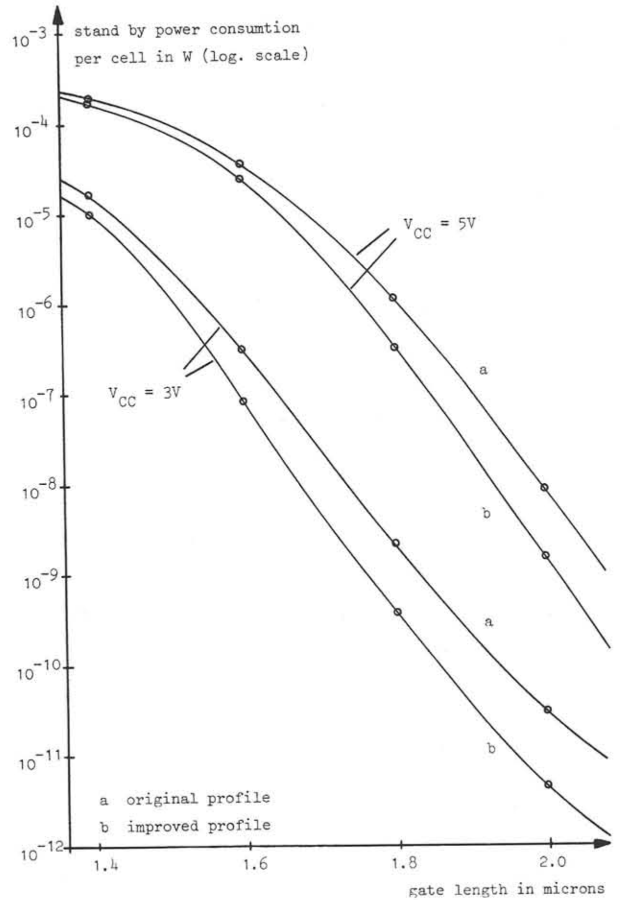

Fig. 8 Stand by power consumtion per cell as function of gate length

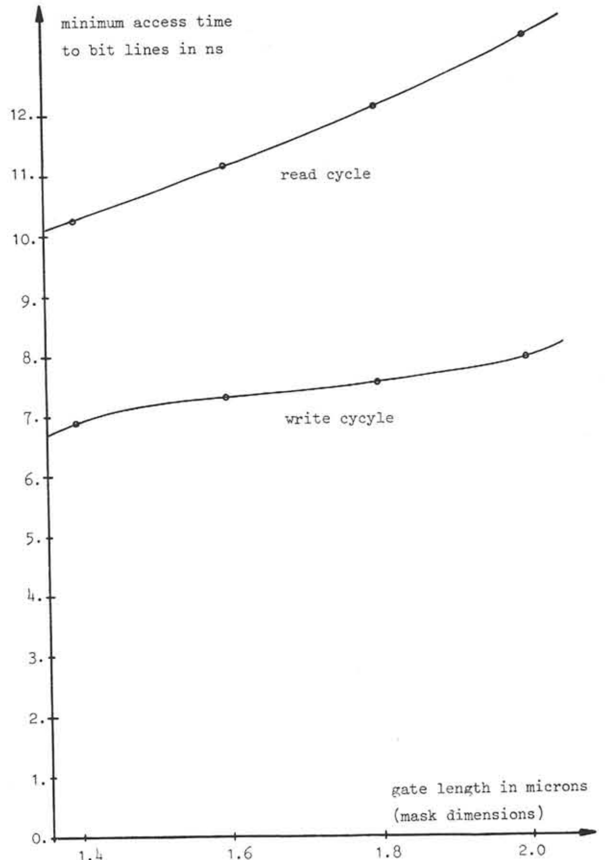

Fig. 9 Minimum access time to bit line as a function of gate length