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Realization of Four-Valued Logic Circuits by NMOS Devices

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A new method to implement four-valued circuits using NMOS devices is proposed. We have designed a simplified elementary form of inverter and various logic circuits, and fabricated several fundamental circuits such as inverter, NAND, NOR and delta literal by the conventional NMOS technology. The features of the present circuits are a small number of comprising MOS transistors, a simple structure and an exact transfer characterisics. Comparisons between the measured and calculated results indicate a good agreement except for some back bias effect.

1. Introduction

There has been a marked increase in the scale and packing density of VLSI. As the number of devices in a VLSI chip increases, the interconnection between active devices inside and outside a silicon chip becomes remarkably complicated and the area percentage occupied by interconnections increases rapidly. Nowadays the occupied area of interconnections is more than 70% of a chip area. In this situation, there has been a continuous interest in the possibility of multiple-valued logic, MVL. The major advantages expected from MVL are (1) reduced interconnection, (2) decreased number of bonding pads and packing pins, and (3) increased packing density[1), 2)].

Up to the present, the implementation of MVL has been studied by using various devices such as I^2L[3)], ECL[4)], CCD[5)], CMOS[6)], NMOS[7)] and MESFET[8)]. NMOS devices are superior in high speed and high density and so are used more than any other device in the binary circuits. However, only a few theoretical studies on MVL circuits using NMOS devices have been reported, which have been restricted to ternary logic circuits.

In this paper, a new method to implement quaternary (four-valued) circuits using NMOS devices is proposed. We have designed an elenental form of circuit and realized various fundamental logic circuits.

2. Design of quaternary logic circuits

The implementation of arbitrary unary functions is indispensable to constructing MVL circuits[9)]. The quaternary unary function is composed of $256(=4^4)$ kinds. A generalized form of the quaternary unary circuits is presented in Fig.1. The input part of this circuit is a delta literal circuit. The circuit comprises E-mode MOST's with four or three kinds of threshold voltages and one kind of D-mode MOST's. The value of $V_T(0.5)$ indicated in Fig.1 means a threshold voltage between voltages of logic level "0" and "1". The values of $V_T(1.5)$ and $V_T(2.5)$ mean the same, as well. The other kind of MOST's, in which the threshold voltage is not fixed, can have any threshold voltage between $V_T(0.5)$ and $V_T(2.5)$, but the use of $V_T(0.5)$ is the most desirable for the decrease in the geometrical β ratio (W/L). The output levels appear in accordance with the truth table as shown in Table 1. The output of level "3", corresponding to the power supply voltage V_{DD}, appears in respective input ranges between 0, $V_T(0.5)$, $V_T(1.5)$, $V_T(2.5)$ and V_{DD}. These output lines are connected to the gate electrodes of Tr0 to Tr3 in the output part, which act as switches. In accordance with desired output levels, the connections indicated in Fig.1(b) should be made in the positions of A to D. By using this general form, any desired unary function can be designed.

Figure 2 shows an inverter circuit derived

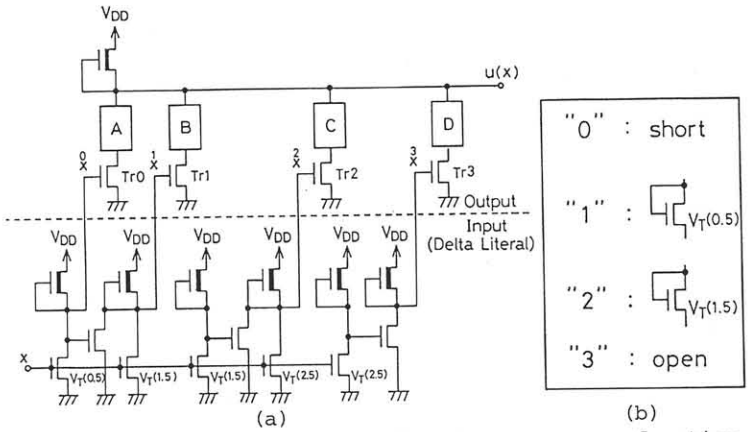


Fig.1 A generalized form of quaternary unary function circuit. Desired connections of A, B, C and D of the output part in (a) are indicated in (b).

from the general form in Fig.1, containing twenty MOST's. If we adopt a priority rule in the appearance of output voltages, the circuit can be remarkably simplified as indicated in Fig.3. This quaternary inverter circuit consists of five E-mode MOST's and one D-mode MOST. The truth table is also indicated in Fig.3(b). The input level is distinguished by three MOST's of T_1, T_2 and T_3 with different threshold voltages, 0.5, 1.5 and 2.5, respectively. On the output stage, voltages of logic levels "0" and "3" are the ground and power supply voltages, respectively. And two intermediate voltages of logic levels "1" and "2" can be obtained by voltage dividers consisting of one D-mode MOST T_0 and one E-mode MOST (T_4 or T_5), connected in series. Figure 4 indicates simulation results of DC transfer characterisics by SPICE-2 using device parameters listed in Table 2. With increasing β ratio of the load MOST T_0 to the driver MOST's (T_1 to T_3), the noise margin increases but the occupied area also increases. Thus, we can easily construct fundamental quaternary circuits simplified using the priority rule of E-mode threshold voltages in the output level.

Various fundamental quaternary logic circuits can be designed on the bases of the above standard form of inverter. For example, NAND and NOR circuits are shown in Figs.5 and 6, respectively. The logic functions of NAND and NOR are also indicated. These circuits have the same input structure as their binary circuits, in which the driver transistors for input are connected in series and parallel, respectively. Both the circuits can be implemented by adding only three

Table 1 Truth table of a quaternary delta literal.

Input	Output			
x	$\overset{0}{x}$	$\overset{1}{x}$	$\overset{2}{x}$	$\overset{3}{x}$
0	3	0	0	0
1	0	3	0	0
2	0	0	3	0
3	0	0	0	3

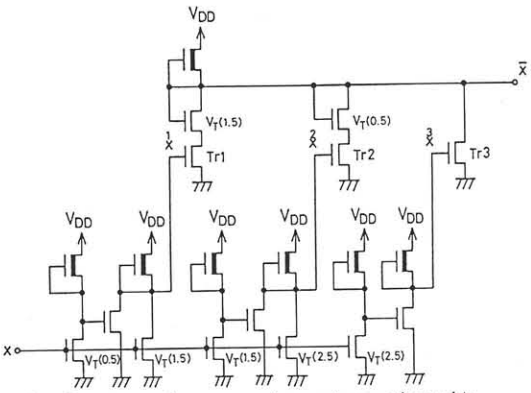
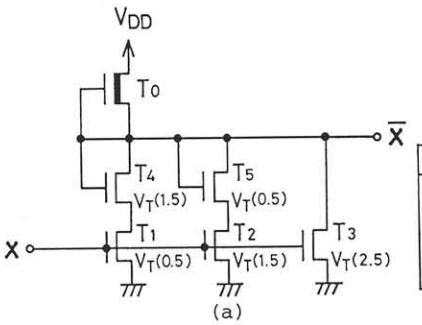
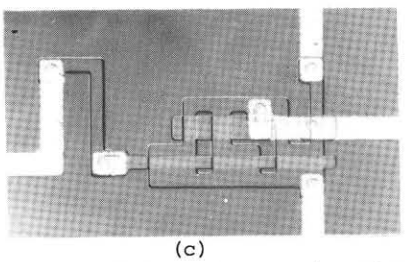


Fig.2 A quaternary inverter circuit derived from the general form in Fig.1.



X	T1	T2	T3	$\overline{X}$
0	OFF	OFF	OFF	3
1	ON	OFF	OFF	2
2	ON	ON	OFF	1
3	ON	ON	ON	0

(b)



(c)

Fig.3 A simplified quaternary inverter circuit: (a) circuit, (b) truth table and (c) optical micrograph.

Table 4 Circuit parameters for the calculation of inverter characteristics (see Fig.3).

Power supply Voltage	V_{DD}: 10.0V
Logic Voltage	0:0.2V, 1:3.5V, 2:6.6V, 3:10.0V
Threshold Voltage (E-mode)	$V_T(0.5)$: 1.5V, $V_T(1.5)$: 4.5V, $V_T(2.5)$: 8.0V
(D-mode)	$V_T(D)$: -3.0V
β Ratio	$(L/W)_{T_0}/(L/W)_{T_5}$: 1.5 $(L/W)_{T_0}/(L/W)_{T_4}$: 1.0 $(L/W)_{T_D}/(L/W)_{T_1,T_2,T_3}$: 4.0, 8.0, 16.0

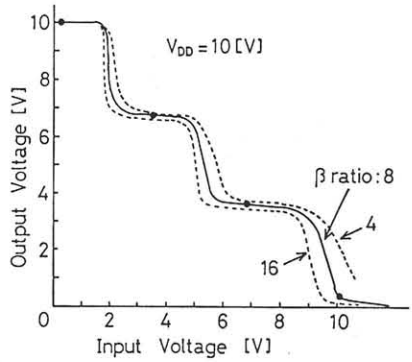


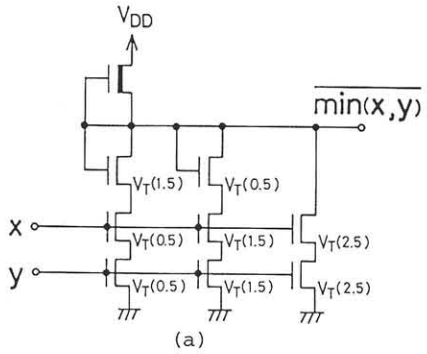
Fig.4 Calculated characteristics of the inverter circuit for three β ratios using parameters listed in Table2.

transistors to the inverter circuit.

At present, it might be difficult that all the circuit constructions are optimized even if a complete set of the functional circuits is provided, because no effective design principle for the quaternary logic system has been found out. However, one of the possible applications in the present state is the following method: The quaternary input signals are decoded into binary signals which are processed using binary logic circuits and then the binary signals are encoded into quaternary output signals. Figure 7 shows a decoder and an encoder circuit for converting binary signals. These circuits are also formed based on the inverter circuit in Fig.3 and can be fabricated by conventional NMOS processes.

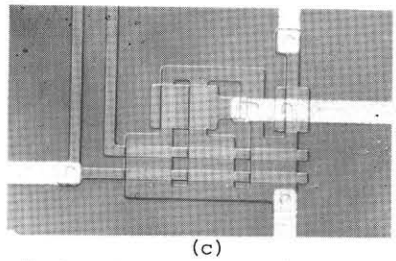
3. Fabrication and evaluation of fundamental logic circuits

The fabrication process was the same as a typical binary NMOS process, adding twice boron implantation to obtain three kinds of E-mode threshold voltages. The process used was a silicon gate NMOS process containing the local oxidation technique. Five times of ion implantations were carried out; one for field region with boron, three for E-mode threshold voltages with boron and one for D-mode threshold voltage with phosphorus. The field oxide was grown at 1000°C by LOCOS, using a plasma-assisted CVD film of Si_xN_y as an oxidation mask. The gate oxide, ∿0.1μm thick, was formed at 1000°C in dry O_2 ambience. The n^+ doped layers were diffused with phosphorus at 1040°C. Nine photolithgraphy steps were necessary until Al interconnection patterning. Typical device parameters fabricated are listed



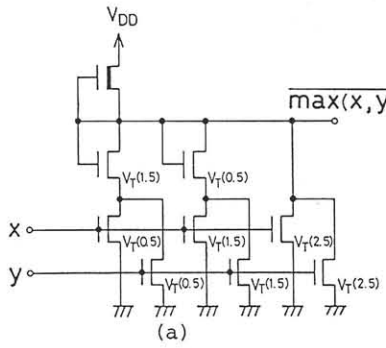
y \ x	0	1	2	3
0	3	3	3	3
1	3	2	2	2
2	3	2	1	1
3	3	2	1	0

(b)



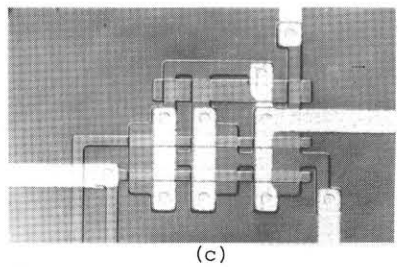
(c)

Fig.5 A quaternary two-input NAND: (a) circuit, (b) truth table and (c) optical micrograph.



y \ x	0	1	2	3
0	3	2	1	0
1	2	2	1	0
2	1	1	1	0
3	0	0	0	0

(b)



(c)

Fig.6 A quaternary two-input NOR: (a) circuit, (b) truth table and (c) optical micrograph.

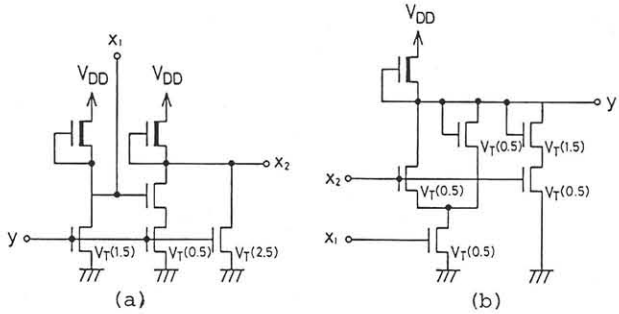


Fig.7 Converters between binary and quaternary signals: (a) decoder and (b) encoder.

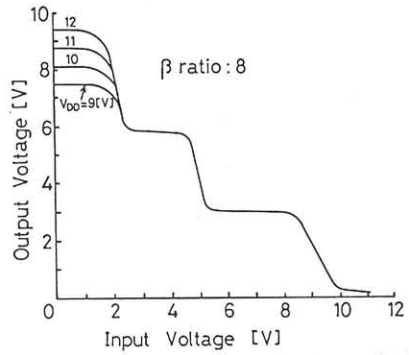


Fig.8 Measured characteristics of the inverter at several power supply voltages.

Table 3 Fabrication process conditions of NMOS devices.

Transistor	E-mode(1)	E-mode(2)	E-mode(3)	D-mode
Ion Implantation	Boron			Phosphorus
Dose (cm^{-2})	$2.5x10^{11}$	$2.0x10^{12}$	$6.3x10^{12}$	$3.2x10^{11}$
Threshold Voltage (V)	1.1	4.2	7.5	-3.5

Substrate: p-type(100), 6∿12Ω-cm
Gate Oxide: 1000∿1100Å

in Table 3. Figures 3(c), 5(c) and 6(c) show optical micrographs of the inverter, NAND and NOR patterns fabricated on a silicon chip. It can be seen that the layout patterns are very simple and correspond well to the each circuit diagram.

Measured characteristics from the inverter in Fig.3 are shown for several power supply voltages in Fig.8. As compared with Fig.4, a good agreement can be seen between both the characteristics, except that the highest output voltage of logic level "3" lowers from the V_{DD}. This lowering is found to become more remarkable with increasing V_{DD} and is attributed to a substrate back bias effect as follows: As the output voltage increases, the pn junctions between substrate and channel regions in the D-mode MOST's are increasingly reverse-biased, and the depletion layer width in the substrate side of the channel region increases. This narrowing of the channel due to the back bias effect results in a decrease in the drain current of D-mode load MOST's and the output (source) voltage cuts off at a value lower than V_{DD}.

One of the possible solutions for this problem is that the implanted impurity profiles in the channel regions of both E-mode and D-mode MOST's are kept remaining near the $Si-SiO_2$ interface as much as possible by using a lower implantation voltage and fabrication temperatures. Another is to lower the power supply voltage. We have been making device parameters optimal and have been designing to realize the desired quaternary logic circuits.

4. Summary

We have proposed a new quaternary circuit system by NMOS devices. These circuits have various advantages suitable for VLSI. The main advantages are a small number of comprising MOST's, simple layout patterns enabling us to make an easy comparison with circuit diagrams, and an exact transfer characteristics. Furthermore, in order to realize more extensively the quaternary circuits the general circuit form of an arbitrary unary function and the decoder and encoder circuits between quaternary and binary logic have also been proposed. The present system has a potential ability of extention and application.

Although the lowering of output voltage has appeared, several improvement ways can be considered: the optimization of device parameters, the realization of a sharp implanted impurity profile in channel regions and the lowering of power supply voltage. At present, we have been placing an effort on the above-mentioned problem, and various functional circuits have been designed and fabricated.

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