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High Performance EEPROM Using Low Barrier Height Tunnel Oxide

N.MATSUKAWA S.MORITA AND H.NOZAWA

SEMICONDUCTOR DEVICE ENGINEERING LABORATORY, TOSHIBA

KAWASAKI 210, JAPAN

A new simple method to fabricate thin oxide with low barrier height is proposed, which is to grow oxide on heavily implanted silicon substrate with As or P in excess of 5 x $10^{14}/cm^2$. When oxide was grown in H_2O + Ar gas after Ar annealing, barrier height of oxide band with respect to silicon conduction band down to 1.8 eV, which is about one half of the ordinary value of 3.2 eV. This phenomenon is applied to EEPROM, which shows superior writh/erase characteristics. Moderately As implanted (2.5 x $10^{15}/cm^2$) sample shows excellent write/erase endurance over 10^6 cycles with 2 V Vth window, which is hardly realized by using the ordinary oxide.

1. INTRODUCTION

Nowadays high performance and high density electrically erasable PROM (EEPROM) is strongly desired and many trials have been done until to realization of 64K bit and beyond as practical EEPROMs(1). In order to advance higher integration, however, scaling of programing voltage as well as device size scaling will be required, which is accompanied by thinning of tunnel oxide and eventually degradation of its reliability. In fact, scaling of tunnel oxide thickness is limited by leakage of stored charge due to direct tunneling. Its limit seems to be about 60A (2). One way to break through this limitation is to use rather thick material with lower barrier height as an electron injector. Along this concept several efficient electron injectors such as poly-oxide, Si-rich SiO_2 and Si_3N_4 have been investigated. Since, all of them, however, employ CVD method, there are certain problems in controllability and reliability in making a very thin layer.

A new simple method, which can overcome above difficulties, will be described in this paper. An SiO_2 layer, thermally grown on heavily doped bare Si substrate, gives rise to low barrier height, which strongly depends on impurity dose and oxidation atmosphere, but not so strongly on a kind of impurity. This phenomenon may be related to unaccountable barrier lowering of very heavily doped poly-oxide, which has rather smooth surface.

This new method is successfully applied to EEPROM, and moderate impurity dose results in better write/erase endurance.

2. EXPERIMENTAL

Process parameters used under investigation of barrier height lowering are listed in Table 1. After field oxidation, As or P were implanted to bare Si substrate. The As dose was ranged from $5x10^{14}/cm^2$ to $1x10^{16}/cm^2$ and P dose was $1x10^{16}/cm^2$. Some wafers were annealed, prior to thin oxide formation, in Ar + 7%O_2 gas at 1000°C for 30 minutes to increase surface impurity concentration, and then about the oxide grown during annealing was removed. In order to form very thin oxide on the highly doped Si substrate, Ar diluted O_2 or H_2O gas was used at 900°C. After poly-Si deposition, phosphorus was doped at 900°C in 20 minutes.

Oxide thickness was measured by two methods, the optical (elipsometlic) and another, electrical (1MHz C-V), method, both of which showed good agreement. I-V characteristics of thin oxide capacitors with area of $1x10^{-2}mm^2$ were measured by YHP 4140B picoammeter, which was placed in circuit as shown in Fig. 1.

Based on the above mentioned process, EEPROM cells were fabricated as shown in Fig. 2. After patterning the 1st poly Si (floating gate), its surface was oxidized to form the 411A this 2nd gate oxide in Ar+O_2 gas at 1000°C. Finally

control gate was made by the N^+ 2nd poly-Si followed by conventional NMOS process.

Amplified high voltage pulse up to 25V with 10μs rise and fall time, which is needed to suppress undesirable overshoot and undershoot, was applied to EEPROM cell as shown in insets of Fig. 5 to measure write/erase characteristics. The pulse used in write/erase endurance test have the rise and fall time of lms and also lms duration at constant high voltage. Applied voltage was determined to induce the threshold voltage window of about 4V. Data retention tests in the erased state at 300°C was performed after several cyclings for the write/erase test.

3. RESULTS

Barrier height lowering

While the oxide thickness, grown in $Ar+O_2$ is dependence of arsenic implanted dose in the substrate, the one grown in $Ar+H_2O$ is quite sensitive to the dose as shown in Fig. 3.

Figure 3 also shows Fowler-Nordheim plot of I-V characteristics of thin oxides for different thicknesses with three defferent dose. In general, slopes in log I/E^2 vs I/E decrease with increasing As ion dose from $5x10^{14}/cm^2$ to $5x10^{15}/cm^2$. The dominant conduction mechanism of the current is supposed to be Fowler-Nordheim tunneling from the linearity of the plats especially at lower doses. The barrier height ϕ_B can be calculated using equation (1).

$$J/E^2 = C\exp(-B/E);\ B=4(2m_{ox})^{1/2}\phi_B^{3/2}/q\hbar \qquad (1)$$

Impurity dose dependence of ϕ_B is shown in Fig. 4. The barrier height lowering commonly occurs but it tends to saturate, when the dose exceeds $2.5x10^{15}/cm^2$. Oxidation in O_2+Ar gas induces less lowering, but pre-annealing in Ar gas seriously promote this phenomenon. In case of oxidation in H_2O+Ar gas with pre-annealing, barrier is extremely lowered down to 1.8eV, which is about one half of an ordinary value. Phosphorus induces the similar reduction, which may suggest a physical mechanism behined this phenomenon.

EEPROM

Figure 5 shows write/erase characteristics of fabricated EEPROM, which use thin oxide with the lowest barrier height of 1.8eV. In spite of the thick oxide of 225A, a small (20V, lms) voltage pulse results in as large as 4V window, which would be obtained by above 30V pulse using in normal oxide. On the other hand, in spite of low barrier height good data retention characteristics have been obtained as shown in Fig. 6, where the solid curve represents the calculated result by thermionic emission model, in terms of Eq. (2).

$$n(t)/n(0)-\exp(-vt\ \exp(-\phi_B/kT)) \qquad (2)$$

where n(t) is the stored charge at time t and v is the electron-lattice collision frequency (3). Substituting $v=10^3-10^7/s$, obtained from EPROM data, ϕ_B was calculated to be 1.0-1.3eV, which is in good agreement with previously reported values for poly-oxide, 1.0-1.8eV . That is to say, data retention characteristics are determined by the 2nd gate poly-oxide, not by thin tunnelable oxide.

Figure 7 shows write/erase endurance characteristics. Although in highly doped case Vth window rapidly disappears after 10^4 cycles, moderately ion implanted sample, in spite of initial narrowing of its Vth window, shows very prolonged endurance and it maintains 2V window over 10^6 cycles, which is hardly realized by the ordinary oxide (4).

4. DISCUSSIONS

Mechanism

Hypotheses can be proposed to explain this new phenomenon, such as rough asperity, including tiny Si clusters, off-stoichiometric SiO_2 and including clustering impurity. In our SEM photograph asperity larger than 300A was not been observed. The fact that barrier height lowering is promoted by thermal pre-annealing and it is almost independent of a kind of impurity, may suggest a clue to solve the problem. It has been reported that heavily implanted As in excess of solid solubility generates As clusters in Si substrate especially around the projection range during thermal annealing(5). This fact may not contradict with our experimental results, because the clusters will be incorporated into the oxide during thermal oxidation which and supports impurity cluster model providing that the dielectrtic constant of the cluster is higher than of SiO_2. Based on the model, our results are explained as follow. When Si is oxidized in $Ar+O_2$ gas without pre-annealing arsenic or phosphorus precipitate with oxide growth and its

cluster is incorporated into the oxide. The preannealing may promote the precipitation to yield much clusters. Moreover, when $Ar+H_2O$ gas is used to oxidize the substrate deeper until reaching impurity projection range, more clusters can be embeded into SiO_2. Moreover, by adopting this model, the barrier height lowering of oxide grown on both highly doped bulk Si and poly-Si are unifiedly explained, impurities in poly-Si can precipitate more easily at the grain boundaries and induce further barrier height lowering.

In write/erase cycle test, initial narrowing of Vth window, in case of moderate impurity concentration, may be related to high density hole traps, although there is no evidence yet, and further study on the nature and behavior of trap must be done to reveal the origin of the prolonged write/erase endurance.

Future prospect

The barrier height lowering results in the the write/erase voltage lowering, and may cause a certain degradation in retention characteristics which would be limited by tunneling leakage through thin oxide. Figure 8 shows an optimized region where sufficient retention of more than 10 years and a short writing or erasing time of less than 1ms for four different effective floating gate voltages are obtained. In thinner oxide region of less than 60A, retention time is degraded to be shorter than 10 years, due to direct tunneling. With ordinary thin oxide with the barrier height of 3.2eV, the thickness can be allowed to be 60 to 110A at the high effective floating gate voltage, 12V, but at 6V no window is remained for the oxide thickness. On the other hand, when the barrie height is 1.8eV, the thickness of oxide can be allowed to be 100 to 135A even at 6V. This means that the writing and erasing voltage can be reduced to 6V and this technology is very promising for the VLSI applications, where the downward scaling of writing and erasing voltage would be inevitable.

5. CONCLUSIONS

A new simple method to make efficient electron injector, which is to grow oxide on highly doped (implantation of As or P over $5x10^{14}/cm^2$) Si substrate resulting in low barrier height, is proposed. Barrier height lowering tends to be saturated when As dose exceed $2.5x10^{15}/cm^2$ and has strong dependence on oxidation method. Decreasing order of barrier height is O_2+Ar oxidation, anneal + O_2+Ar oxidation, anneal + H_2O+Ar oxidation. The last method can lower the barrier height as small as 1.8eV, which is about one half of the normal value.

This phenomenon was applied to EEPROM to form tunnelable side for a carrier injector. It shows good write/erase characteristics; 4V Vth window with 20V 1ms pulse, in spite of rather thick oxide, and has good data retention characteristics limited by poly-oxide leakage. Moderately As implanted ($2.5x10^{15}$) sample shows very prolonged endurance and it still maintains 2V window over 10^6 cycling which is hardly realized by the ordinary oxide.

The possible model or the barrier height lowering seems to be impurity cluster incorporated into oxide, although there still remains a room to be investigated for more detailed understanding.

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PARAMETERS for THIN OXIDE FORMATION		
Implant Dose	As	0.5, 2.5, 5.0, 10×10^{15}/cm 40KeV
	P	10×10^{15}/cm 35KeV
Ar Anneal	1000°C, 0 or 30min, O_2(7%) + Ar	
Thin Oxidation	900°C, H_2 + Ar, (66A - 225Å)	
	O_2 + Ar, (107 - 147Å)	
Electrode	N+Poly, (P-Diff. 1000°C 20min)	

Table 1. Parameters for thin oxide formation.

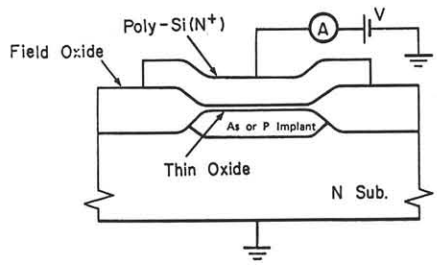

Fig. 1 Schematic representation of thin oxide capacitor with measuring circuit.

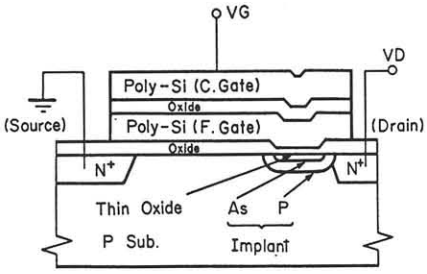

Fig. 2 Schematic representation of EEPROM cell used in this study.

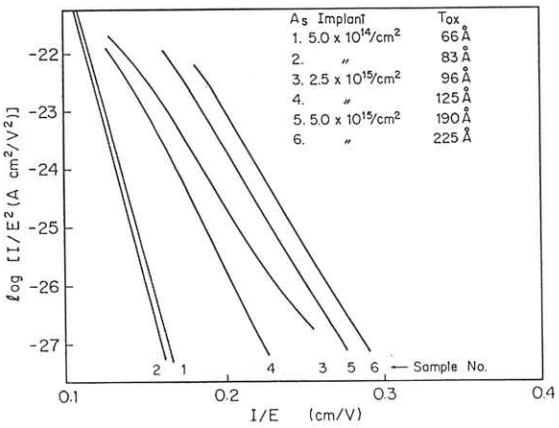

Fig. 3 Fowler-Nordheim plot of I-V characteristics of thin oxide grown on implanted silicon surface in H_2O+Ar gas after Ar annealing.

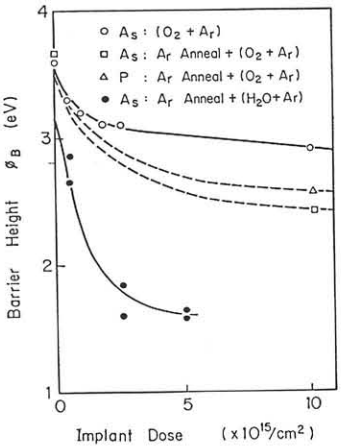

Fig. 4 Impurity dose dependence of the barrier height.

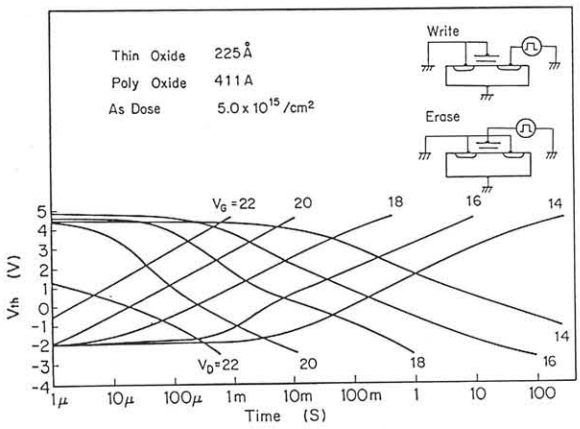

Fig. 5 Write/erase characteristics of EEPROM employing thin oxide with low barrier height (1.8eV).

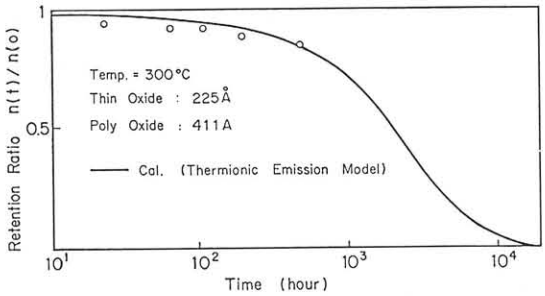

Fig. 6 Data retention characteristics of EEPROM with low barrier height oxide (1.8 eV)

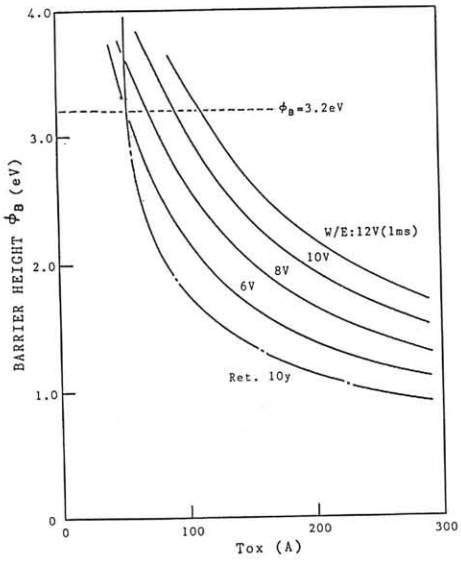

Fig. 8 Optimization of barrier height (ϕ_B) and oxide thickness (Tox) for 10 years retention and 1ms writing and erasing at four different gate voltage.

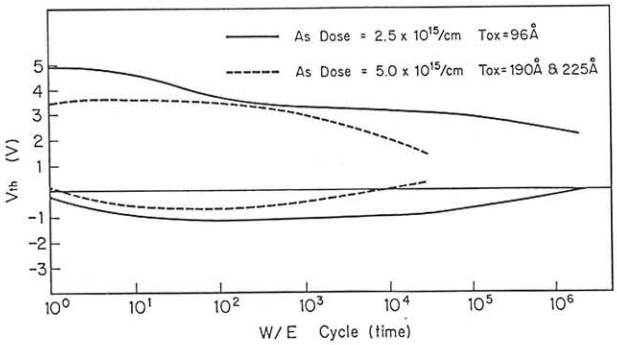

Fig. 7 Write/erase endurance of EEPROM with thin oxide grown in H_2O+Ar gas on heavily implanted (5.0×10^{15} /cm^2) and moderately implanted (2.5×10^{15}/cm^2) Si substrate.