Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 265-268

TITE RAM: A New SOI DRAM Gain Cell for Mbit DRAM's

H. Shichijo, S.D.S. Malhi, A.H. Shah, G.P. Pollack, W.F. Richardson,
M. Elahy, S. Banerjee, R. Womack, and P.K. Chatterjee

Semiconductor Process and Design Center
Texas Instruments Inc.
P. O. Box 225621, MS 369
Dallas, Texas 75265

A new DRAM gain cell using SOI LPCVD polysilicon MOSFET is proposed and experimentally demonstrated. This cell can realize a cell size of less than 15 um^2 with 1 um design rules for Mbit level MOS dynamic RAMs. Because the signal storage region is isolated by oxide, the cell is expected to be immune to soft errors and substrate disturbances. Typical signal retention times of 10 - 50 msec at room temperature, and 1 - 5 msec at 100 C are obtained.

1. INTRODUCTION

As the density of MOS dynamic RAMs reaches Megabit levels, the design of DRAMs using a conventional one-transistor cell (1-T cell) encounters increasing difficulties. The cell size requirement inhibits the use of a large capacitor which is necessary for a sufficient noise margin. The decreasing signal also makes the cell more susceptible to soft errors and minority carrier disturbances from the substrate. One possible remedy is to use a trench capacitor(1) in the conventional 1-T cell configuration. However, the advantage of such a structure and its scalability in terms of soft errors and substrate disturbances are not clear. 1-T DRAM cell built in beam-recrystallized polysilicon on oxide(2,3), on the other hand, eliminates the soft errors, but still suffers from the capacitor size constraint for proper signal sensing.

Another approach which has been pursued is the use of a cell which has an internal gain for signal readout(4,5). This eliminates the cell size constraint due to the capacitor size. However, the gain cells proposed up to now all require three logic levels which makes the design of the peripheral circuits very difficult. They also store the signal charge in bulk silicon.

In this paper, a new DRAM cell having both advantages, oxide isolation of the stored charge and the internal readout gain, is proposed and demonstrated. The cell also utilizes simple two level logic and a standard 5V power supply. This cell has been named the TITE (Transverse Injected Two Electrode) RAM cell.

2. CELL STRUCTURE AND OPERATION

The cell described here stores the signal charge on a polysilicon node which forms the gate electrode of the bulk sense transistor. The structure of the proposed cell and its equivalent

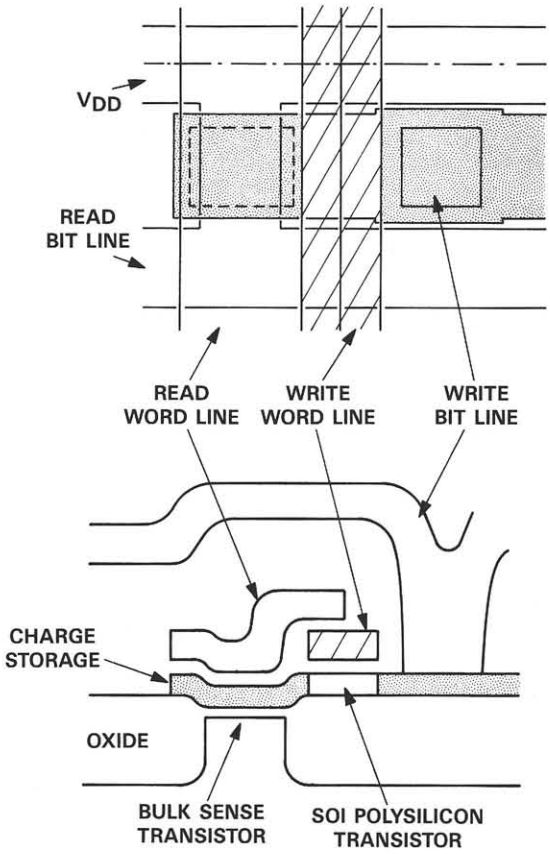

Fig. 1 TITE RAM cell structure.

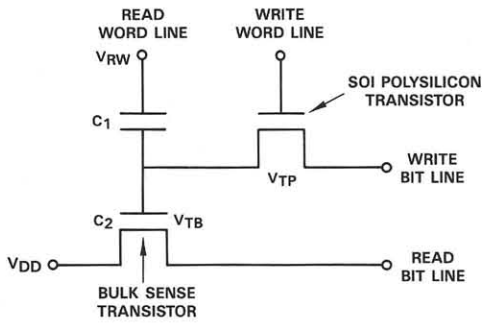

Fig. 2 Equivalent circuit for TITE RAM Cell

circuit are shown in Figs. 1 and 2, respectively. The cell consists of a MOSFET built in LPCVD polysilicon on oxide(6) and a conventional bulk MOSFET. Both MOSFETs are n-channel devices, and the channel of the polysilicon MOSFET can be either p-type doped, undoped, or lightly n-type doped(7).

The cell is configured with two word lines and two bit lines. During a write operation, both the read word and write word lines are held high at a positive voltage allowing the data "1" or "0" on the write bit line to be written into the storage node through the polysilicon FET. After the write operation, the write word line first returns to 0V, which electrically floats the charge storage node. Then, the read word line returns to 0V. This causes the storage node to make a negative transition through the capacitance coupling. A sufficient coupling will lower the potential of the "1" written node to below the threshold voltage of the bulk sense transistor so that this transistor is turned off during the standby for both "1" and "0" written cells. The read operation is done by bringing only the read word line high. Again through the capacitive coupling, this brings the storage node potential to above the threshold voltage of the sense transistor for the "1" written cell, but brings it only to 0V for the "0" written cell. Therefore, the sensing current for "0" is much less than that for "1", distinguishing the two states.

3. CELL DESIGN

In order to maximize the signal output while minimizing the standby current, the coupling efficiency of the read word line voltage to the polysilicon storage node needs to be optimized. This efficiency is determined by the capacitance ratio between the top capacitance (C_1) and the total gate oxide capacitance of the bulk sense transistor (C_2) including the gate overlap capacitance.

Although C_2 actually depends on the on/off state of the sense transistor, it is assumed to be constant here in order to simplify the discussion. Then, the following two conditions are required.

1) During the store (or hold) state, the sense transistor must be off for both "1" written and "0" written cell. The read word line is high (at V_{RW}) during the write and read operations, and is low (at 0V) during the store. Thus, the amount of capacitive coupling is $C_1/(C_1 + C_2)V_{RW}$. Assuming the voltage written on the storage node is V_H when the read word line is high, the condition above requires

$$V_H - C_1/(C_1 + C_2)V_{RW} < V_{TB} \qquad (1)$$

where V_{TB} is the threshold voltage of the bulk sense transistor. 0V on the "0" written cell is coupled down to $- C_1/(C_1 + C_2)V_{RW}$.

2) If the coupling coefficient is large, the node voltage on the "0" written will go negative far enough during the store operation to turn on the polysilicon transistor because its gate is held at 0V. In other words, if $-C_1/(C_1 + C_2)/V_{RW} < - V_{TP}$, the polysilicon transistor is turned on, and the signal leaks out. Therefore, the most negative voltage on the node is $- V_{TP}$ during the store. When this node is coupled up during the read, it should not exceed V_{TB} for the maximum signal difference for "1" and "0". In other words,

$$- V_{TP} + C_1/(C_1 + C_2)V_{RW} < V_{TB} \qquad (2)$$

must be satisfied. From (1) and (2), the capacitance ratio must be within the range such that

$$V_H - V_{TB} < C_1/(C_1 + C_2)V_{RW} < V_{TP} + V_{TB} \qquad (3)$$

is satisfied.

4. EXPERIMENTAL RESULTS

An experimental 2X2 test array has been fabricated using 4 um design rule to demonstrate the cell concept. A double level polysilicon process with both the read and write word lines on the same second polysilicon level is used for process simplicity. Fabrication of the polysilicon transistor has been described

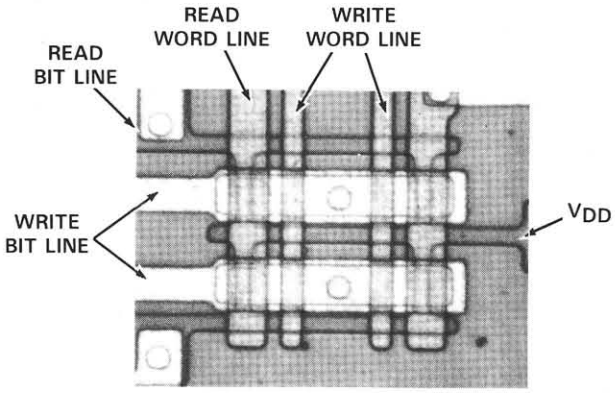

Fig. 3 Photograph of 2x2 TITE RAM cell.

previously(5). Figure 3 shows a photograph of 2x2 test array.

The voltage waveforms of Fig. 4 confirm the operation of TITE RAM cell. The threshold voltage of the bulk sense transistor is approximately 2V. The output current of the sense transistor is monitored through a 10 Kohm external resistor connected to the read bit line. The "1" readout current is approximately 50 uA while the "0" readout current is negligible (<1nA).

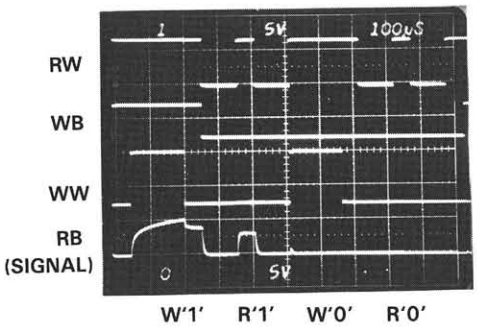

Fig. 4 Voltage waveforms for 2x2 TITE RAM cell array.

RW = Read word line

WB = Write bit line

WW = Write word line

RB = Read bit line

Figure 5 shows the effect of varying the read word line voltage, and therefore the coupling voltage, on the output signal. The smaller read word line voltage results in a smaller voltage coupling. Therefore, the relation (1) is not satisfied anymore, and the node voltage during the "0" store is above V_{TB}. This causes the output signal during "0" store to increase sharply.

Similarly, Fig. 6 shows the effect of the read word line voltage on the signal retention time of "1" and "0" states. The signal retention time is determined by the signal leakage through the polysilicon transistor during the store. For a "1" written cell, only a drain bias is applied to the polysilicon transistor because the read word and write bit lines are held at 0V. For "0" written cell, on the other hand, the storage node potential is negative, and both the drain and

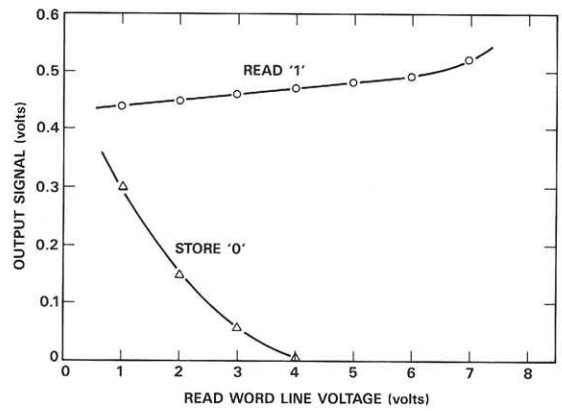

Fig. 5 Readout current versus read word line voltage in read "1" and store "0" operations.

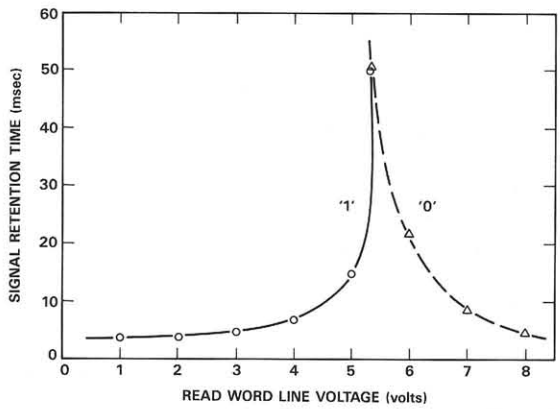

Fig. 6 Signal retention time versus read word line voltage for "1" and "0" written cells.

gate biases are applied. For a small read word line voltage (and a small coupling voltage), the node potential during the "1" store is high, and a high drain bias exists which increases the leakage for the "1" written cell, thus reducing the "1" signal retention time. For a large read word line voltage, on the other hand, the node potential during the "0" store is more negative which increases the leakage for the "0" written cell. Therefore, an optimum capacitance coupling exists which maximizes the signal retention time for both "1" and "0" as illustrated in Fig. 6. Similar relations have been obtained at 100 C operation. At optimum read word line voltage, a signal retention time of more than 5 msec has been obtained at 100 C. Typically, the retention time at 100 C is a factor of 30 - 50 smaller than that at room temperature. This temperature dependence is related to the leakage property of polysilicon transistors(7). This small ratio is in contrast to the value of approximately 1000 for the conventional 1-T cell(8).

5. CONCLUSIONS

The operation of the TITE RAM cell has been described. Since the signal charge is isolated by oxide, the cell reduces the susceptibility to soft errors and minority carrier disturbances. Also, the internal gain of the cell eliminates the cell size limitation due to the capacitor size. Using 1 um design rules, the cell size of less than 15 um^2 can be realized.

The capacitive coupling coefficient is shown to be an important parameter for the optimization of the signal difference for "1" and "0" and the signal retention time. The maximum signal retention time of more than 50 msec at room temperature, and more than 5 msec at 100 C has been demonstrated. The smaller temperature dependence of signal retention time compared to a conventional 1-T cell is related to the leakage current of polysilicon transistor. Unlike other gain cells, this cell operates with a standard 5V power supply and simple two level logic. All these features make the TITE RAM cell very attractive for Mbit level DRAMs.

ACKNOWLEDGEMENT

The authors acknowledge the excellent assistance and support from all members of the Semiconductor Process and Design Center.

REFERENCES

(1) H. Sunami, T. Kurie, N.Hasimoto, K. Itoh, T. Toyabe and S. Asai, IEDM Tech. Digest, P.806, 1982.

(2) R. D. Jolly, T. I. Kamins and R. H. McCharles, IEEE Elect. Dev. Lett., EDL-4, 8, 1983.

(3) J. C. Sturm, M. D. Giles and J. F. Gibbons, IEEE Elect. Dev. Lett., EDL-5, 151, 1984.

(4) P. K. Chatterjee, G. W. Taylor, R. L. Easley, H-S. Fu, and A. F. Tasch, Jr., IEEE Trans. Elect. Devices, ED-26, 827, 1974.

(5) T. Tsuchiya and S. Nakajima, IEEE Trans. Elect. Devices, ED-29, 1713, 1982.

(6) S.D.S. Malhi, R. R. Shah, P. K. Chatterjee, H. W. Lam, R. F. Pinizzotto, C. E. Chen, H. Shichijo and D. W. Bellavance, DRC Tech. Digest, paper VB-1, 1983.

(7) H. Shichijo, S.D.S. Malhi, P. K. Chatterjee, R. R. Shah, M. A. Douglas and H. W. Lam, IEDM Tech. Digest, P. 202, 1983.

(8) J. E. Leiss, P. K. Chatterjee and T. C. Holloway, IEEE Trans. Elect. Devices, ED-29, 707, 1982.