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Uniformity of In-Alloyed LEC GaAs

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Crystals of In-alloyed GaAs made by the LEC method exhibit nonuniformities arising from the segregation of In and from changes in metal/As stoichiometry in the melt during growth. Growth from an As-rich melt leads to good electrical uniformity of as-grown material. Crystallographic uniformity is greatly increased by the dislocation-suppressing effect of In alloying.

§1. Introduction

Crystals of In-alloyed GaAs made by the liquid-encapsulated Czochralski method can have many fewer dislocations[1)] than unalloyed LEC GaAs without losing their desirable semi-insulating (SI) electrical properties for application as direct implantation substrates.[2,3)] We have prepared In-alloyed GaAs[4)] for use in studies in our laboratory[5,6,7)] on the relationship between substrate dislocations and the electrical behavior of arrays of MESFETs made by a direct ion implantation process. In these studies it was shown that FET threshold voltage does not depend on the distance from the FET to the nearest dislocation, in contrast to published reports for GaAs substrates.[8)] In the work reported here, we have examined crystals of In-alloyed GaAs with special attention to crystallographic and compositional properties that might influence the uniformity of electrical behavior of FETs fabricated on In-alloyed GaAs substrates.

§2. Segregation of In

The distribution coefficient of In between crystalline and liquid GaAs is 0.118,[4)] so that the melt becomes richer in In as growth proceeds. This causes a progressive increase in In concentration from the seed to the tail of the crystal, and necessitates slow pull rates (we used 4 mm/hr) to avoid constitutional supercooling and cellular growth. A crystal grown at 6 mm/hr from a melt containing 6 atom percent of In became polycrystalline at the tail, presumably because of the onset of cellular growth.

Another effect of the segregation of In is the appearance of growth striations as seen in the x-ray topograph of Fig. 1. The ring features represent local variations of In concentration (and lattice constant) as the plane surface of a wafer cuts across the traces of the nonplanar growth interface. The pattern of the rings shows that the growth interface is somewhat bumpy rather than plane or concave or convex. The wafer, of composition $In_{0.0063}Ga_{0.9937}As$, was from the seed end of the crystal for which etch pit patterns are given in Fig. 2.

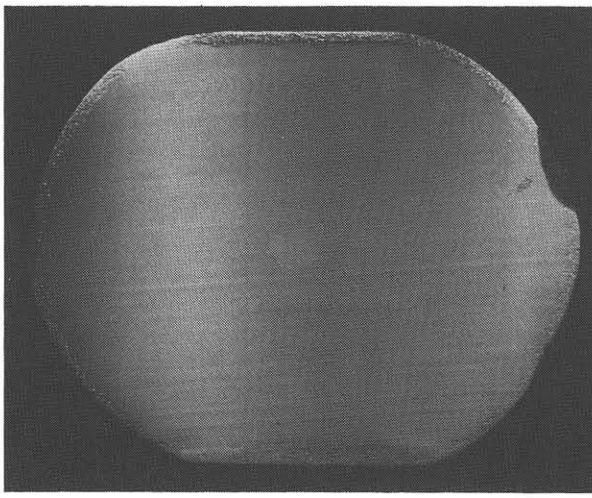

Fig. 1 X-ray topograph of (100) wafer cut normal to the growth axis of a crystal of $In_{0.0063}Ga_{0.9937}As$.

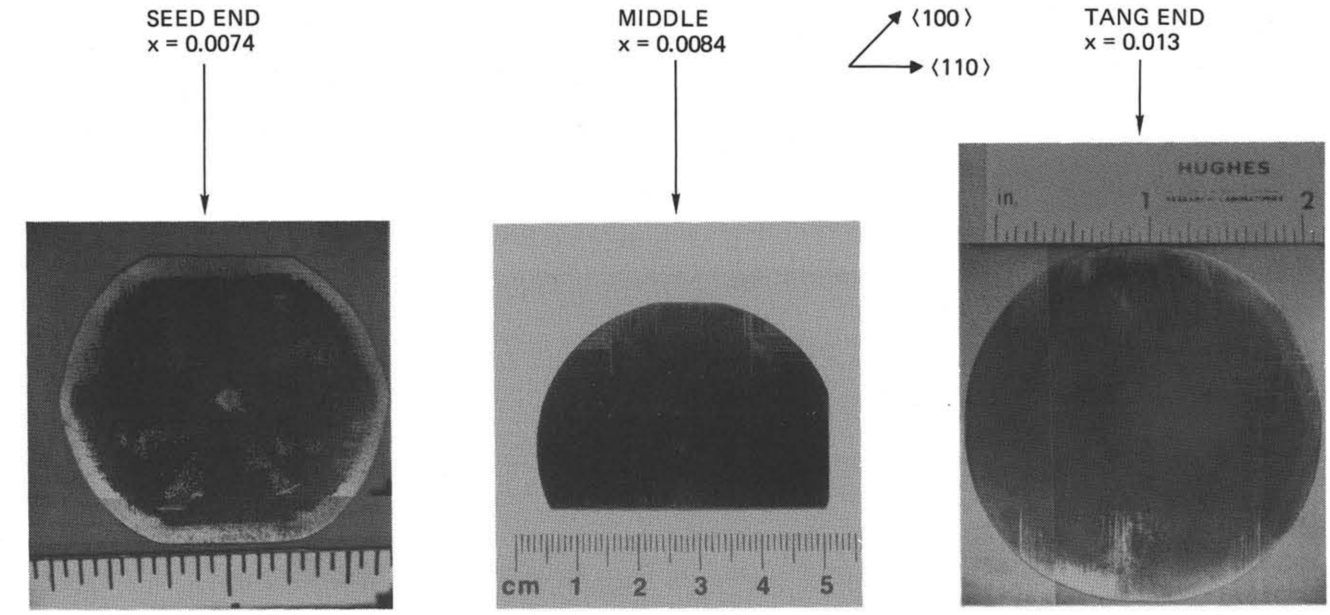

Fig.2. Etch pits revealed by molten KOH in wafers from near the seed, the middle, and the tail of an In-alloyed crystal grown from an As-rich melt. The value of x in In_xGa_{1-x} is given for each wafer.

§3. Dislocations

With increasing In concentration, the crystal becomes more resistant to the generation and propagation of dislocations by thermal stress. An example is provided by the KOH etch patterns shown in Fig. 2 for wafers from near the seed, the middle, and near the tail of an In-alloyed GaAs crystal. (The x-ray topograph of Fig. 1 is for a wafer still closer to the seed end of the same crystal.) Near the seed, the dislocations occur in a rosette pattern aligned along the <100> directions. Vestiges of the rosette pattern can be seen by examining the actual etched middle and tail wafers, although it is not visible in the reproductions in Fig. 2. The wafer from the middle of the crystal is the one most nearly dislocation-free. The tail-end wafer, despite its higher In content, exhibits a greater density of dislocations arrayed in lines along <110> directions near its periphery. These relationships are shown more quantitatively in Fig. 3, which shows that all three wafers have a peak in dislocation density at their centers, with the lowest peak occurring in the middle wafer. The absence of any observable dislocations at the edges of the middle wafer in Fig. 3 probably results from that part of the crystal having been ground down to a two-inch diameter. Fig. 2 shows some typical slip lines along the upper edge of the middle wafer; the diameter along which the etch pit density counts of Fig. 3 were made runs from left to right, thus missing the upper edge with its dislocations. The electrical properties of this crystal appear in Table I.

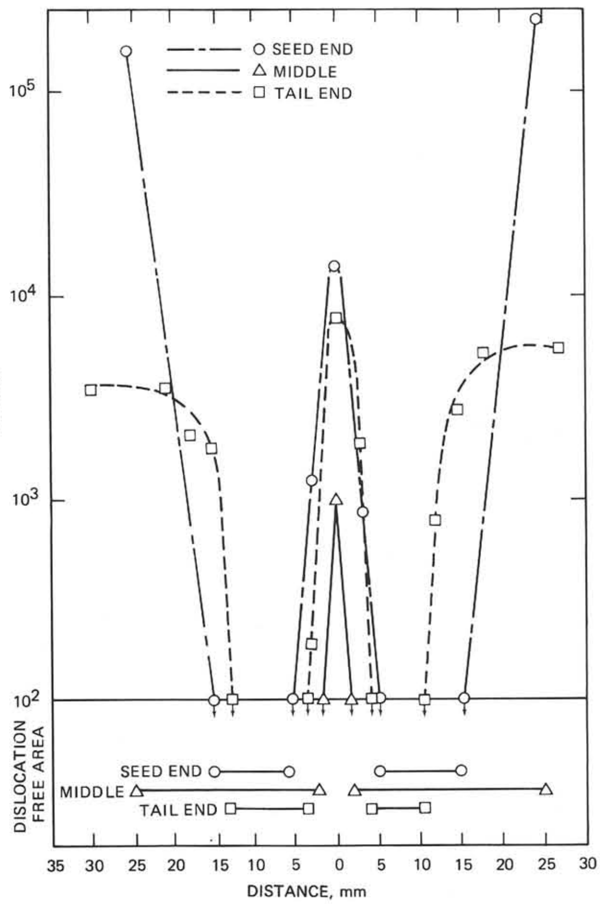

Fig. 3 Plots of etch pit density along a <110> diameter for the three wafers of Fig. 2.

Table I. Room temperature electrical properties of 6-mm-square samples cut along <110> diameters of wafers from ingots grown from an As-rich melt.

Sample Number	ρ ohm-cm	n cm^{-3}	μ cm^2-V^{-1}-s^{-1}
Seed-1	2.54_8	4.10_6	6216
Seed-2	2.21_8	4.46_6	6343
Seed-3	1.36_8	7.42_6	6204
Seed-4		Not measured	
Seed-5	2.34_8	4.23_6	6294
Tail-1	1.03_8	9.46_6	6399
Tail-2	1.02_8	9.11_6	6723
Tail-3	1.02_8	8.84_6	6943
Tail-4	8.79_7	9.94_6	7142
Tail-5	7.44_7	1.28_7	6531
Tail-6		Not measured	
Tail-7		Not measured	
Tail-8	8.05_7	1.24_7	6251
Tail-9	1.12_8	8.44_6	6574

§4. Electrical Properties

In agreement with the well-known effects of melt stoichiometry[9] on undoped LEC GaAs crystals grown in PBN crucibles, we find that when the initial melt is As-rich the crystal is SI throughout. With an As-rich initial melt, the uniformity of electrical properties across wafers of the as-grown SI material is excellent. In Table I we list room-temperature resistivity, mobility, and carrier concentration for samples taken along diameters of seed and tail wafers of a crystal grown from an As-rich melt. Measured resistivities are almost all above 10^8 ohm-cm and mobilities all above 6200 cm^2-$volt^{-1}$-sec^{-1}. The tail wafer has significantly higher carrier concentrations and mobilities than the seed wafer.

When the melt is slightly As-deficient initally, it becomes more so during growth and the tail of the crystal becomes low-resistivity p-type[3,4] just as in the case of unalloyed undoped GaAs.[9] Wafers from the SI portion of such a crystal do not have as uniform carrier concentrations and mobilities as wafers from As-rich melts. Table II shows that, for a wafer close to the seed end of a crystal from an As-deficient melt, the center Hall sample is electrically similar to the seed samples of Table I for a crystal from an As-rich melt. However, there is a pronounced drop in mobility for the edge sample. Also listed in Table I are Hall results for a wafer near the position at which the crystal turned low-resistivity p-type. The edge sample has a drastically reduced mobility, and the center sample, while still of high resistivity, exhibited p-type behavior, as well as pronounced anisotropy in the resistivity measurements. Low n-type mobilities and anisotropic resistivities are often observed in GaAs samples that have very rapid spatial variation of the Fermi level as the result of close (but spatially varying) compensation between deep donors and net acceptors. Just such a situation occurs near the SI p-type boundary in a crystal grown from an As-deficient melt.

Table II. Center and edge room-temperature Hall results for wafers from a crystal grown from an initially As-deficient melt.

	ρ ohm-cm	n cm^{-3}	μ cm^2-V^{-1}-s^{-1}
Seed Center	1.52_8	6.02_6	6289
Seed Edge	2.21_8	5.23_6	5398
Middle* Center	1.92_7	8.36_8	390 (p-type)
Middle* Edge	2.34_8	8.64_6	3092

*Wafers after this were low-resistivity p-type.

§5. Discussion

Some of the nonuniformities in In-alloyed undoped GaAs crystals are shared with unalloyed crystals: a transition from SI to p-type behavior for crystals grown from As-deficient melts, and variations in carrier mobility across wafers taken from SI regions close to the SI-p-type transition. We have presented an x-ray topograph of an In-alloyed crystal wafer that clearly shows the existence of striations. While the contrast of the topograph is due to the variations of In concentration, the mechanisms that cause the observed striations may be expected to cause local variations in residual impurities and in grown-in defect densities. Thus we can take the striations observed in In-alloyed GaAs as evidence for the probable existence of striations in unalloyed GaAs as well.

It is desirable to avoid As-deficient melts in growing both unalloyed and In-alloyed GaAs for substrates, in order to keep the crystals SI throughout their length. The data of Tables I and II suggest another benefit; mobilities and carrier concentrations of as-grown material are much more uniform across the wafer for a crystal grown from an As-rich melt than for one from an As-deficient melt.

The long-range segregation behavior of In has specific effects on the variations of properties along an In-alloyed LEC crystal. The concentration of In rises from seed to tail. The dislocation density at first decreases from the seed toward the tail, as the In concentration increases. For the crystal of Figs. 1, 2, and 3, the dislocation density reached a minimum and then rose slightly toward the tail. We suggest that increasing thermal stresses at the tail end of the crystal outweighed the dislocation-suppressing effect of increasing In concentration.

Previous work in this laboratory[6,7] has shown that the threshold voltage (V_{th}) of a FET is independent of the FET's proximity to a dislocation for both unalloyed and In-alloyed GaAs substrates. While there appears to be a correlation between local average V_{th} and local average dislocation density for GaAs substrates with 10^4 to 10^5 dislocation cm^{-2}, no such correlation is observed for In-alloyed GaAs substrates with dislocation densities from less than 10^2 to 10^4 cm^{-2}.[6,7] The local uniformity of V_{th} was best in the lowest-dislocation regions of an In-alloyed substrate, with a standard deviation of 0.010 V for 24 FETs in a 0.5 mm^2 area.[6] Nevertheless, the mechanisms for the influence of substrate dislocations on FET V_{th} remains obscure. The dislocation-suppressing effect of In makes the alloyed crystals much more uniform crystallographically than unalloyed material. We expect that the availability of In-alloyed GaAs with very low dislocation densities will make it possible to study the effects of single isolated dislocations on implant activation and FET properties.

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