

Homogeneity Improvement of LEC-Grown, Semi-Insulating GaAs by Heat-Treatment

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Heat-treatment of conventional LEC-grown, semi-insulating GaAs wafers at 800°C for more than 12 hr resulted in improving crystal inhomogeneities related to dislocations. The improvement was confirmed by measuring MESFET threshold voltage standard deviation σV_{th} . σV_{th} for long term annealed substrates exhibited one half that for a nonannealed substrate. Photoluminescence study suggested that shallow acceptor like defects might be redistributed, which act as a "killer" center for Si ions being donors.

1. Introduction

GaAs integrated circuits have recently developed increasingly by means of the direct ion implantation into semi-insulating GaAs substrates. Liquid-encapsulated Czochralski (LEC) grown, undoped and/or low Cr doped semi-insulating GaAs crystals are now currently used as the substrates.

However, an LEC grown GaAs crystal generally includes high dislocation density ranging from a low 10^4 cm^{-2} to more than mid 10^5 cm^{-2} , and the density exhibits a W-shaped variation across a (100) wafer. Extensive studies on electrical and optical homogeneities have been collectively correlated to the the macroscopic W-shaped dislocation density variation¹⁻⁹). Particularly, it has been clearly observed that threshold voltage for MESFET is strongly influenced by dislocations. More recently, the authors have also found that a long term heat-treatment of the wafer prior to the ion implantation provides the improvement of crystal inhomogeneities related to dislocations¹⁰).

This paper reports extended results of the heat-treatment effect on homogeneity improvement of LEC-grown, undoped and low Cr doped substrates. Evident improvement was verified by measuring a standard deviation of threshold voltage for MESFETs fabricated on wafers. The results on photoluminescence and

cathodoluminescence studies were also presented so as to explain the improvement.

2. Experiments

The substrates used in this study were prepared from a direct synthesis LEC-grown, undoped and low Cr doped, semi-insulating 2 inch diameter crystals. A thickness of one-side polished wafer was $450 \pm 20 \mu\text{m}$. The wafers were heat-treated at 800°C for 8 - 32 hr, with about 1500 Å thick pCVD SiN cap film on both side, in a resistance furnace in flowing N_2 . Followed by the annealing, about 50 μm thick surface layer was polished away (referred as treated wafer), considering the well-known Cr pile-up toward the wafer surface and the out-diffusion of deep level EL-2. Semi-insulating characteristics for the treated wafers was then confirmed by two-probe leakage current measurement. Some samples were etched with molten KOH in order to clarify whether dislocation density varied or not. It was noticed that dislocation density and its distribution exhibited no significant alteration even after the long term annealing.

Homogeneity improvement was finally verified by measuring a standard deviation of MESFET threshold voltage. Conventional FETs with 6 μm source-drain distance, 5 μm gate width and 1 μm gate length were fabricated on Si implanted

and annealed wafers. Si dose was $2.0 \times 10^{12} \text{ cm}^{-2}$ at 60 KeV and the activation annealing was performed at 800°C for 20 min. with a SiN cap. Moreover, sheet carrier concentration in the active surface layer was also examined with a conventional van der Pauw method.

For evaluating the homogeneity improvement, cathodoluminescence (CL) at near bandedge emission was observed at room temperature and also photoluminescence (PL) study was carried out at 4.2K.

3. Results and discussion

Figure 1(a) shows CL images for different treated wafers. Usually, CL image gives speckled bright regions, which is corresponding to dislocation clusters. When the heat-treatment was provided, CL bright region

around dislocations became broader in accordance with the increasing periods. Figure 1(b) shows typical CL line scanned intensity variations. Less than about 9 hrs. heat-treatment, a lot of fine peaks were observed, which is closely correlated to dislocation clustered cell networks. With the increase in the annealing period, CL fine peaks disappeared with increasing background intensity. The CL bright region around dislocations is sometimes referred to as a "denuded" zone, which is "depleted" of some shallow acceptor impurities or point defects¹⁰. Then, inhomogeneities related to dislocation distribution might be reduced to some extent by more than 12 hrs heat-treatment. It is worth speculating that CL intensity homogeneity might be due to thermal diffusion and/or redistribution of impurities and/or point defects.

Wafer homogeneity was verified by measuring (i) standard deviation $\langle V_{th} \rangle (1 \times 24)$ for about 600 FETs located on a $1 \times 24 \text{ mm}^2$ stripe area along the $\langle 110 \rangle$ axis and (ii) standard deviation $\langle V_{th} \rangle (5 \times 5)$ for 625 FETs on a $5 \times 5 \text{ mm}^2$ area, which is comparable to actual IC chips. Table I summarizes the measured standard deviation values for several wafers, with an average threshold voltage, $\overline{V_{th}} (1 \times 24)$. It can be noticed that an evident improvement in electrical homogeneity was obtained. The nontreated substrate showed 90-110 mV of $\langle V_{th} \rangle$. This large deviation is caused by high dislocation density and its distribution in as-grown state reported earlier¹⁰. With increasing the annealing period, the standard deviation for both undoped and Cr doped substrates reached about one half that of the nontreated wafer. Figure 2 compares the distribution of threshold voltage across the 110 direction for the nontreated and 24 hr treated, undoped substrates. The nontreated substrate exhibits a so-called M-shaped variation closely correlated to dislocation density distribution, while the treated substrate shows more uniform distribution lying between 0 to -100 mV, which is about one half that for the nontreated substrate. Therefore, it can be concluded that the homogeneity was evidently improved.

Moreover, one notes that the average

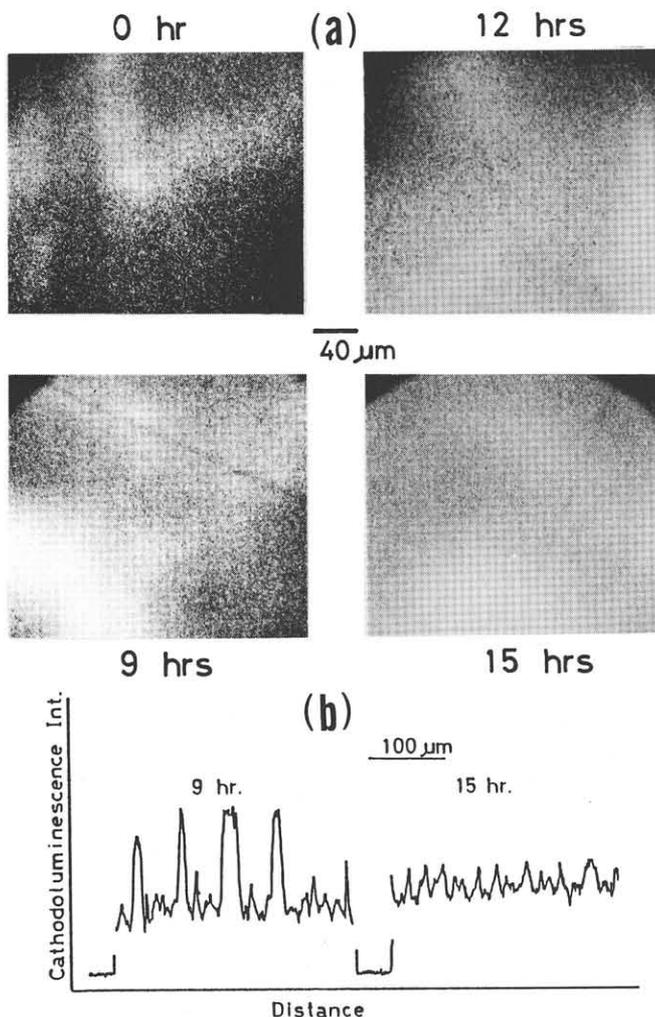


Fig.1 (a) Cathodoluminescence (CL) images for different treated substrates, and (b) line scanned CL intensity variations for 9 and 15 hrs treated substrates.

Table I Measured threshold voltage and standard deviation

Period (hr)	Undoped			Cr doped		
	$\overline{V_{th}}$ (1x24) (V)	σV_{th} (1x24) (mV)	σV_{th} (5x5) (mV)	$\overline{V_{th}}$ (1x24) (V)	σV_{th} (1x24) (mV)	σV_{th} (5x5) (mV)
0	+0.044	119	99	+0.126	101	87
8	+0.042	101	94	-----	---	--
10	-----	---	--	-0.035	64	67
14	-----	---	--	-0.069	50	48
16	+0.032	76	74	-----	--	--
18	-----	--	--	-0.165	41	54
24	-0.067	59	63	-----	--	--
32	-0.130	69	50	-----	--	--

threshold voltage $\overline{V_{th}}$ (1x24) shift toward a normally-on value, as the annealing period increased. This implies that the activation efficiency for implanted Si ions became higher. Then, sheet carrier concentration N_s was measured for Si implanted active layer. The measured results are shown in Fig.3 as a function of the annealing period. It is obviously shown that the activation efficiency (N_s/Φ , Φ = dose, $2.0 \times 10^{12} \text{ cm}^{-2}$) increased with the annealing period. The increase in N_s may be closely correlated with the increase in CL background intensity as was depicted in Fig.1(b).

Photoluminescence study was carried out for evaluating the increase in N_s . For this purpose, the substrate was prepared from a bulk ingot which had already annealed at 800° for 24

hrs. after the growth. For bulk-annealed substrates, the increase in N_s was also confirmed. Figure 4 shows measured PL spectra around bandedge for Si implanted active surface layer and substrate backside (denoted as bulk). Full and dotted curves are corresponding to bulk and Si implanted layer, respectively. The numbers #133-0 and 133-4 mean the nontreated and 24 hr treated substrates, respectively. It can be noticed that the PL spectrum for Si implanted sample without treatment exhibits a broad band

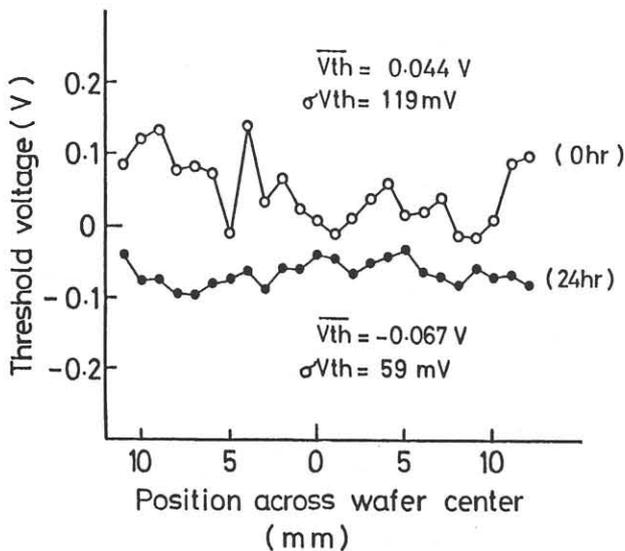


Fig.2 Threshold voltage distributions for nontreated and 24 hrs treated, undoped substrate.

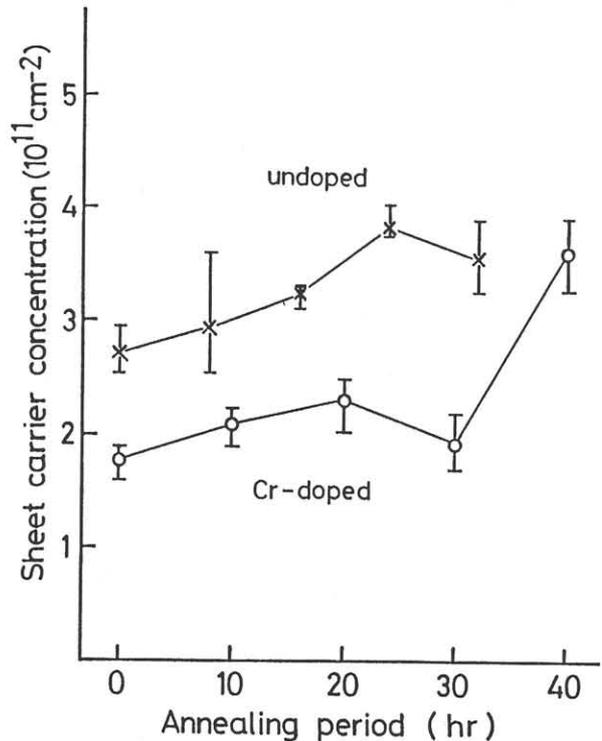


Fig.3 Sheet carrier concentration depending on annealing period at 800° . Si dose was $2.0 \times 10^{12} \text{ cm}^{-2}$.

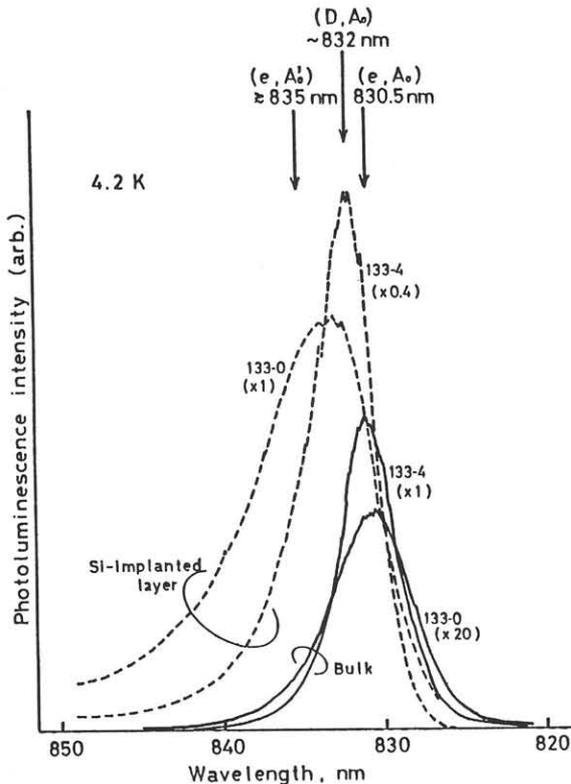


Fig.4 Photoluminescence spectra for Si implanted active layer and backside bulk surface. #133-0 and #133-4 give nontreated and 24 hrs treated substrates, respectively.

consisting of ~ 832 nm and ≥ 835 nm peaks, which are thought to be due to $\text{Si}_{\text{Ga}}(\text{D})-\text{C}_{\text{As}}(\text{A}_0)$ transition and conduction band and $\text{Si}_{\text{Ga}}(\text{D})-\text{Si}_{\text{As}}(\text{A}'_0)$ transition, respectively. On the other hand, the spectrum for the treated and Si implanted sample(#133-4) shows sharp and intense 832 nm emission. Si in As site acts as acceptor. Therefore, it can be said that the high activation efficiency for the treated substrate may be attributable to the decrease in 835 nm emission intensity, that is, when the long term annealing is carried out, As vacancies which act as a sink of implanted Si ions as well as a killer center for donors decreases effectively and allowed high sheet carrier concentration. The PL intensity for deep level EL-2, ~ 0.65 eV, was obtained to be not varied significantly with the annealing period.

From the preliminary results on PL measurements, it can be speculated that shallow acceptors like defects may be eliminated or redistributed by the heat-treatment, resulting in improvement of electrical homogeneity. More detailed investigation is required.

4. Summary

A long term heat-treatment at 800° for conventional LEC grown GaAs substrates was found effective and useful in improving crystal inhomogeneities associated with dislocations. A standard deviation of threshold voltage for MESFETs fabricated in heat-treated substrates reached about one half that for the nontreated one. Although dislocation-free, semi-insulating GaAs crystals are strictly demanded, the long term heat-treatment of wafers prior to IC processes makes applicable available LEC grown substrates contained high dislocations for future development of high performance GaAs LSIs.

The authors would like to express their thanks to Drs. M.Ohmori, K.Wada and K.Hoshikawa for their fruitful discussions, and also to S.Shibata for the cathodoluminescence experiments.

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