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Low Temperature Fabrication of SOI-MOSFET's in Si/CaF_2/Si Heteroepitaxial Structures

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The epitaxial growth of Si films on CaF_2/Si heteroepitaxial structures and characteristics of MOSFET's fabricated in the Si/CaF_2/Si structures are investigated. Both the growth of the Si/CaF_2/Si structures and the fabrication of MOSFET's are performed at temperatures below 800°C. For the growth of Si films, a new growth method, which involves *in situ* deposition of a thin(≤10nm) Si onto the CaF_2 surface at room temperature prior to deposition of Si at elevated temperatures, has been developed in order to prevent interfacial reaction between deposited Si and underlying CaF_2. Al gate n-channel MOSFET's, which are electrically isolated from the substrates, have been fabricated by utilizing plasma enhanced CVD SiO_2 as the gate insulator. The maximum field effect mobility of about 180cm^2/V·s has been obtained.

1. Introduction

Crystalline Si films on composite insulator/Si structures(SOI's) are of great interest not only in dielectric isolation of devices in conventional integrated circuits(IC's), but also in fabrication of three dimensional IC's. Particularly, for the fabrication of three dimensional IC's, the process temperature is desirable to keep low in both processes of SOI formation and device fabrication in order to avoid deformation of dopant impurity profiles and to minimize thermal stresses of the materials. One promissing approach to the formation of SOI's with large-area single crystal Si films at lower temperatures is the heteroepitaxial growth of insulator and Si films. Up to the present heteroepitaxial SOI structures by use of $MgO{\cdot}Al_2O_3$,[1,2] CaF_2,[3-5] and Al_2O_3[6] have been reported. Among these crystalline dielectric materials, the use of CaF_2 is attractive because stoichiometric CaF_2 films can be easily obtained by vacuum deposition and it provides a low temperature process(below 800°C) for the epitaxial growth of both insulator and Si films.

In this presentation, we report fundamental characteristics of SOI-MOSFET's fabricated in the Si/CaF_2/Si heteroepitaxial structures at temperatures below 800°C. For the growth of Si films on CaF_2/Si structures a new growth method, which involves *in situ* deposition of a thin Si layer onto the CaF_2 surface at room temperature prior to the growth of Si at elevated temperatures, has been developed in order to prevent interfacial reaction between deposited Si and underlying CaF_2.[7] Al gate n-channel MOSFET's are fabricated in the Si film on the CaF_2/Si structure by utilizing plasma enhanced CVD SiO_2 as the gate insulator.

2. Growth of Si/CaF_2/Si Structures

2.1 Growth Method

Both (111) and (100) oriented Si wafers were used as substrates. They were chemically cleaned and loaded in a vacuum system having a base pressure of less than $1x10^{-6}$Pa. CaF_2 was first evaporated from a resistively heated crucible at a rate of about 1nm/sec onto the (111) and (100)Si kept at 800°C and 600°C, respectively. These substrate temperatures were so chosen as to obtain single crystalline CaF_2 films with smooth surfaces.[8] CaF_2 films were 150-400nm in thickness. After the CaF_2 deposition, the temperature of the sample was decreased to room temperature(RT) and a thin Si layer was deposited on top of the CaF_2/Si structure. Si was evaporated from an e-gun at a rate of about 0.1nm/sec. The thickness of the thin Si layer was varied from 4 to 32nm. Then the temperature of the substrate was elevated to 700-800°C, and Si deposition was continued. The final thickness of the Si film was 400-500nm. Pressures in

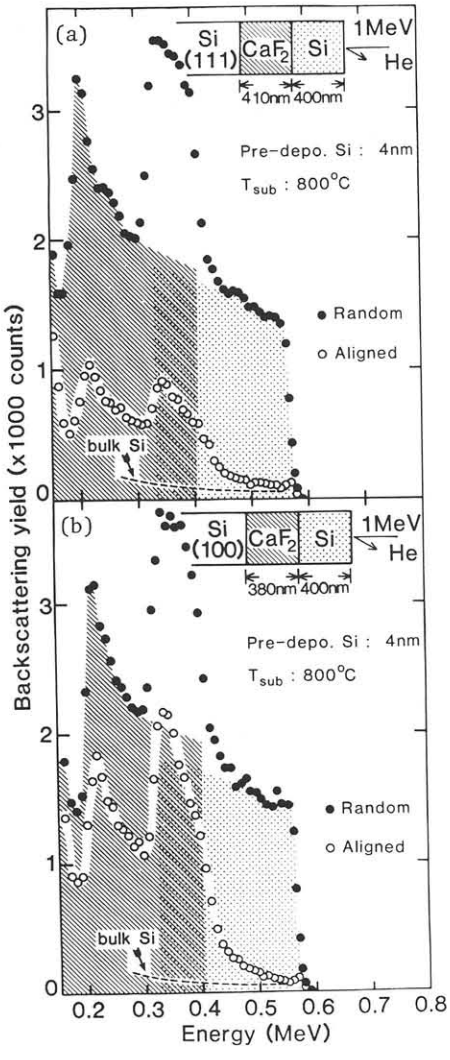

Fig. 1 Random and aligned backscattering spectra of 400nm thick Si films grown at 800°C on CaF_2/Si(111)(a) and CaF_2/Si(100)(b) structures predeposited with 4nm thick Si layers at room temperature. These spectra were taken with 1MeV $^4He^+$ ions.

the chamber were less than $3x10^{-5}$Pa and $1x10^{-4}$Pa during the deposition of CaF_2 and Si, respectively.

2.2 Characterization

Figure 1 shows Rutherford backscattering random and aligned spectra of Si films grown on the CaF_2/Si(111) and CaF_2/Si(100) structures by the thin Si layer predeposition method. In these samples, 4nm thick Si layers were deposited at RT prior to deposition of 400nm thick Si films at 800°C. The random spectra in Fig. 1 show the formation of uniform 400nm thick Si films. We can see from the aligned spectra in Fig. 1 that the Si films grow epitaxially on both (111) and (100) oriented substrates even though 4nm thick Si layers

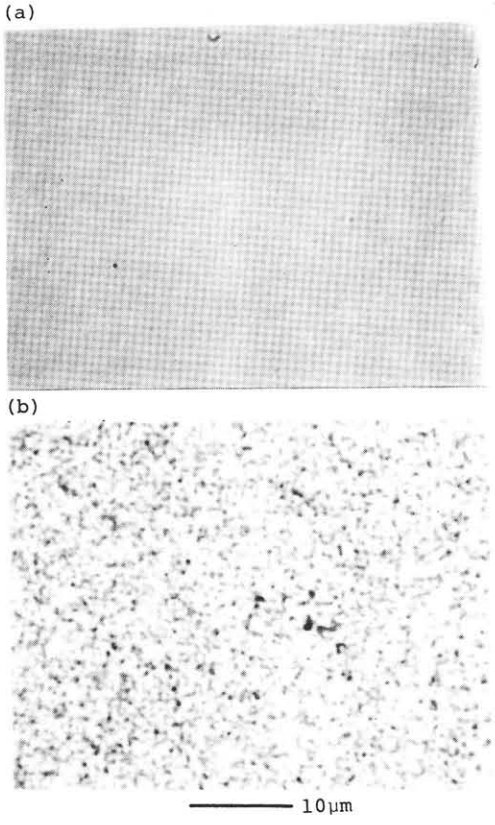

Fig. 2 Optical micrographs of surfaces of Si films grown at 800°C on CaF_2/Si(111) structures with a 4nm thick predeposited Si layer(a) and without a predeposited layer(b).

were predeposited at RT onto the CaF_2 surfaces. The channeling minimum yield χ_{min} (the ratio of the aligned yield to the random yield) of the Si film on the (111) substrate is about 21% near the interface, and it reduces to about 7% near the surface. In the case of the Si film on the (100) substrate, the χ_{min} near the interface is about 67%. But it is markedly reduced toward the surface, and the χ_{min} near the surface is about 6%.

Figure 2(a) shows the surface morphology of the same sample that shown in Fig. 1(a) observed by a Nomarski interference microscope. In Fig. 2(b), the surface morphology of a 90nm thick Si film directly grown at 800°C onto a CaF_2/Si(111) structure without the predeposited Si layer is shown for comparison. The surface of the Si film grown without the predeposited layer is rough, which might result from reaction between deposited Si and underlying CaF_2. Crystalline quality of this Si film was poor(χ_{min}>50%). On the contrary, as shown in Fig. 2(a), the surface of the Si film grown by the predeposition method is uniform, exhibiting little surface relief. The Si film

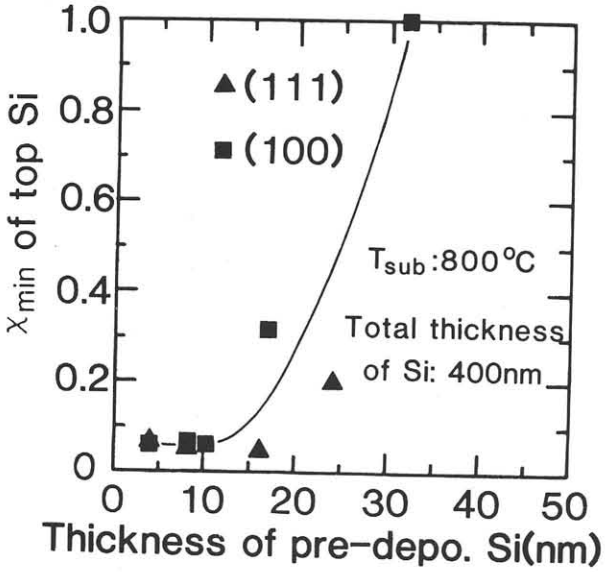

Fig. 3 Variation of the near surface χ_{min}'s of 400nm thick Si films grown on CaF_2/Si structures with thickness of predeposited Si layers. Si films were grown at 800°C.

grown on the CaF_2/Si(100) structure with the predeposited layer showed a similar smooth surface to that shown in Fig. 2(a)

Figure 3 shows the variation of the near surface χ_{min} of approximately 400nm thick Si films on (111) and (100) substrates with thickness of the predeposited Si layer. Si films were grown at 800 °C. No particular difference in these plots can be observed between (111) and (100) substrates. The χ_{min}'s of Si films on both (111) and (100) substrate are less than 8% when the predeposited Si layer is about 10nm or less in thickness. However, the increase of thickness of the predeposited Si layer results in degradation of the crystalline quality of Si films. From these results, we can say that the thin(≤10nm) Si predeposition method is useful to prevent the interfacial reaction between deposited Si and underlying CaF_2 without destroying the epitaxial growth of Si films on CaF_2/Si structures.

3. Characteristics of MOSFET's

3.1 Fabrication Process

Al gate n-channel MOSFET's were fabricated in the Si/CaF_2/Si structure grown by the predeposition method. Figure 4 shows a schematic cross-section of a MOSFET. MOSFET's were fabricated at temperatures below 800°C by the following process.

1) A Si/CaF_2/Si(100) structure was prepared by

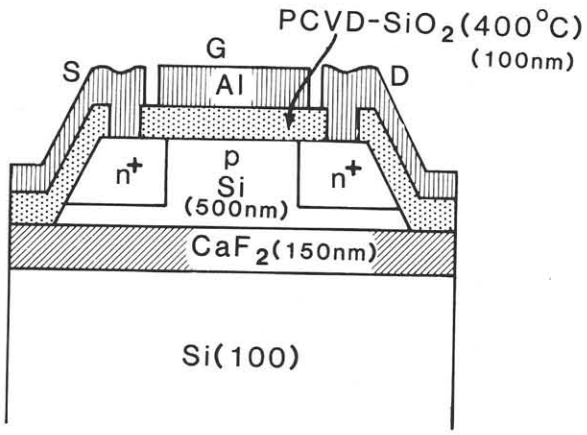

Fig. 4 Schematic cross-section of a MOSFET fabricated in the Si/CaF_2/Si structure.

growing a 150nm thick CaF_2 film at 600°C and a 500 nm thick Si film at 750°C. A 5nm thick Si layer was predeposited onto the CaF_2 surface. Backscattering measurements showed that the channeling minimum yield in the Si film was about 13% near the surface.

2) The channel doping was performed by implanting 50keV and 100keV B^+ ions in whole area of the sample to doses of $5\times10^{11}cm^{-2}$ and $8\times10^{11}cm^{-2}$, respectively. After that, 50keV P^+ ions were implanted in the source and drain regions to a dose of $1\times10^{15}cm^{-2}$.

3) FET regions were defined in island forms by etching of the Si film with CF_4 plasma. It has been confirmed that complete selective etching of Si is possible by CF_4 plasma.[4)]

4) In order to electrically activate implanted species, the sample was annealed at 800°C for 30 min in vacuum.

5) For the gate insulator, a 100nm thick SiO_2 film was deposited at 400°C by PCVD of SiH_4+H_2+N_2O system. Prior to the deposition of SiO_2, the sample was immersed in N_2O plasma for 5min in order to remove contaminants from the surface. The capacitance-voltage measurement of MOS diodes fabricated on a single crystal Si(100) wafer by this method showed that the density of interface states was about $5\times10^{11}cm^{-2}$.

6) Electrodes were formed by vacuum deposition of Al.

3.2 Fundamental Characteristics

Figure 5 shows drain current vs. drain voltage characteristics of an as-prepared MOSFET which has a channel length of 35μm and a channel width

of 20μm. The field effect electron mobility derived from these characteristics is about 110cm^2/V·s. Figure 7 shows a drain current vs. gate voltage characteristic at a drain voltage of 10(V). The subthreshold leakage current between the source and the drain is about $2x10^{-8}$(A)(10^{-9}A/μm). The leakage current between the source or the drain and the substrate was in the range of 10^{-12}-10^{-10}A.

In order to improve the drain characteristic of the MOSFET's, the sample was annealed at 400°C for 20min in vacuum. The drain characteristic was improved by this annealing process, and the field effect mobility of about 180cm^2/V·s was obtained.

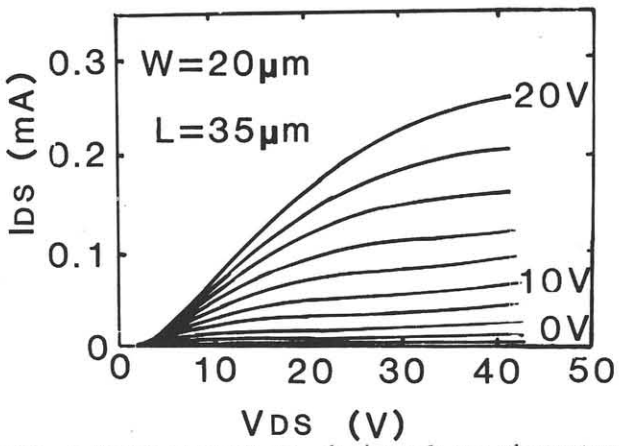

Fig. 5 Drain current vs. drain voltage characteristics of an as-prepared MOSFET with a channel length of 35μm and a channel width of 20μm.

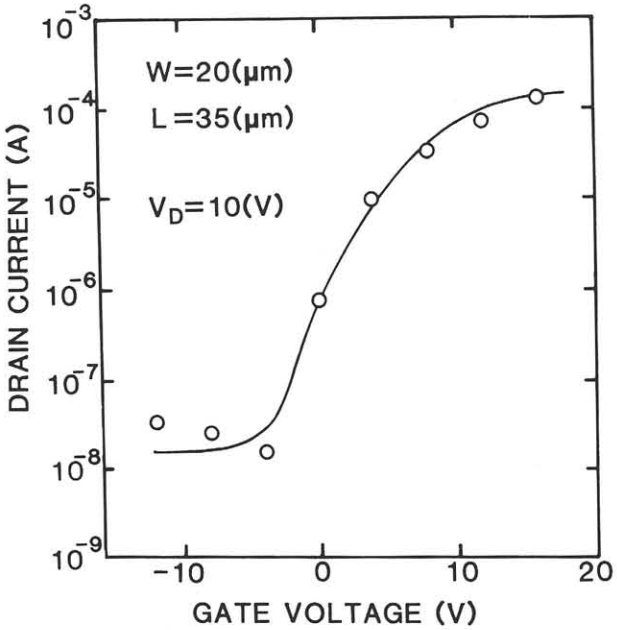

Fig. 6 Drain current vs. gate voltage characteristic at a drain voltage of 10(V) of the same FET that shown in Fig. 5.

4. Summary

We have investigated the growth of Si/CaF_2/Si heteroepitaxial SOI structures and the fundamental characteristics of MOSFET's fabricated in the Si/CaF_2/Si structures by low temperature process. The following summarize this work.

1) By the use of the thin(≤10nm) Si predeposition method, the interfacial reaction between deposited Si and underlying CaF_2 can be prevented without destroying the epitaxial growth of Si. Consequently we can obtain uniform Si films of better crystalline quality than Si films grown by conventional direct deposition of Si onto CaF_2/Si structures.

2) MOSFET's, which are electrically isolated from substrates, can be fabricated in the Si/CaF_2/Si structures. By the use of a PCVD SiO_2 films deposited at 400°C as the gate insulator, the maximum field effect electron mobility of about 180cm^2/V·s was obtained.

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(References)

1) M. Ihara, Y. Arimoto, M. Jifuku, T. Kimura, S. Kodama, H. Yamawaki, and T. Yamaoka: J. Electrochem. Soc., 129(1982)2569
2) M. Mikami, Y. Hokari, K. Egami, H. Tsuya, and M. Kanamori: Ext. Abs. 15th Conf. Solid State Devices and Materials, Tokyo, 1983, p. 31
3) H. Ishiwara and T. Asano: Appl. Phys. Lett., 40(1982)66
4) T. Asano and H. Ishiwara: Proc. 13th Conf. Solid State Devices, Tokyo, 1981, Jpn. J. Appl. Phys. 21(1982)Suppl. 21-1, p. 187
5) T. Asano and H. Ishiwara: Thin Solid Films, 93(1982)143
6) K. Takahama and A. Hanabusa: Digest of the 1983 Spring Meeting of the Jpn. Soc. Appl. Phys. and Related Soc., Chiba, 1983, 7p-N-10, p. 523
7) T. Asano and H. Ishiwara: J. Appl. Phys., 55(1984)3566
8) T. Asano, H. Ishiwara, and N. Kaifu: Jpn. J. Appl. Phys., 22(1983)1474