Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 523-526

B-10-3

MOSFET Characteristics of Connected Silicon Islands on Fused Silica

Yutaka Kobayashi and Akira Fukami

Hitachi Research Laboratory, Hitachi, Ltd.

Hitachi, Ibaraki, 319-12, Japan

Aluminum gate, n channel MOSFETs were fabricated on isolated and connected silicon islands which were recrystallized on fused silica substrate using an RF-heated zone melting recrystallization method. The field effect mobility of the device fabricated on the connected silicon island was about 900 cm^2/Vs, which was twice that of the device fabricated on the isolated island, while its leakage current was 10^{-13} A/μm, which was two orders lower. These observations were attributed to the realization of (100) oriented single crystal silcon and the decrease in positive charge density at the silicon-fused silica interface. A 51 stage EE MOSFET ring oscillator was also fabricated on the connected islands. Its propagation delay time was 2.2 ns, which was three times faster than that of bulk silicon.

1. Introduction

Silicon on a fused silica substrate structure has many advantages when used for display devices such as active liquid crystal displays and high speed integrated circuits. The structure can be produced by melt regrowth methods using beams[1,2,3] and carbon heaters[4,5]. However, a difference in the thermal expansion coefficient between silicon and fused silica causes cracks in the silicon layer, and the crystalline quality of the recrystallized silicon is difficult to control because a seeding technique cannot be applied to the structure.

The authors previously reported on an RF heated zone melting recrystallization method, in which cracks in the recrystallized silicon on fused silica were eliminated by forming islands[6]. It was found that the polycrystalline silicon must have characteristics like connected silicon islands with fine regions in order to obtain high quality crystalline silicon without cracks and with an orientation of (100)[7].

This report investigates improvements of crystalline quality and device characteristics obtained by recrystallizing the connected polycrystalline silicon islands on fused silica.

2. Recrystallization of connected silicon islands

The expansion coefficient of fused silica is one order lower than that of silicon, so cracking appears in recrystallized silicon formed on fused

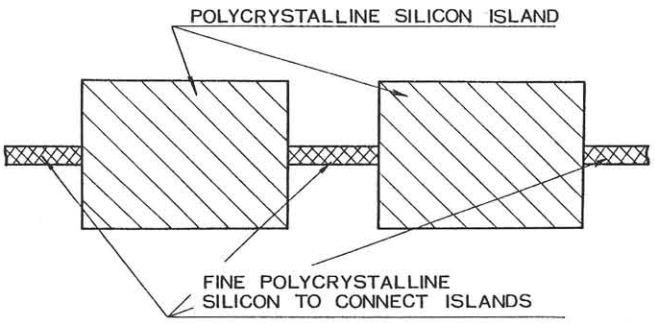


Fig.1 Connected silicon island structure

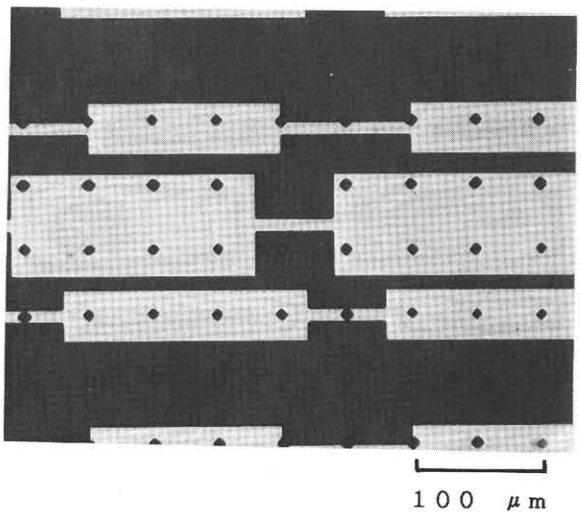


Fig.2 Orientation of recrystallized silicon islands which are connected with fine silicon region.

silica. When MOSFETs are fabricated on a silicon layer that contains cracks, the characteristics of the devices are abnormal. Cracking is eliminated by forming islands before recrystallization.[2,6,7] In this method, however, the silicon is recrystallized from a supercooled state and its orientation is (111).[6,7] In order to obtain high quality silicon and to fabricate a high speed switching MOSFET, recrystallization from the supercooled state must be avoided and (100) oriented silicon must be obtained.

Based on these considerations, a recrystallization method of connected silicon islands was proposed.[7] The structure is shown in figure 1. Silicon was formed as an island to eliminate cracking and islands were connected to each other with fine polycrystalline silicon to achieve a smooth heat flow. Then the polycrystalline silicon was recrystallized.

Details of the process are as follows. A 0.75 μm thick polycrystalline silicon film, which was deposited on an optically polished fused silica substrate, was etched to form connected island shapes. The wafer was covered with a 1.2 μm thick silicon dioxide layer. Then the polycrystalline silicon was recrystallized using an RF heated zone melting recrystallization method (RF-ZMR). The high temperature region was at 1450 °C. Wafer traveling speed was 0.5 mm/s.

Figure 2 shows the crystal orientation of silicon recrystallized by this method. The orientation was studied with the etch pit method.[8] The shape of the etch pits was square, confirming orientation of the recrystallized silicon as (100). The rotation angles were all the same in an island, hence it was a single crystal.

Figure 3 shows the defect etched silicon surface. In these figures, the melted silicon region moved from left to right during the recrystallization. As shown in figure 3 (a), a sub-boundary appeared in the end region of the island, however there was none on the front side. This meant that the sub-boundary could be eliminated in the whole island area if the width of the connecting regions and the area of the islands were optimized. Figure 3 (b) shows an example in which the sub-boundary was eliminated. The island was 50 μm wide and 100 μm long. The width of the connecting region was 2.5 μm.

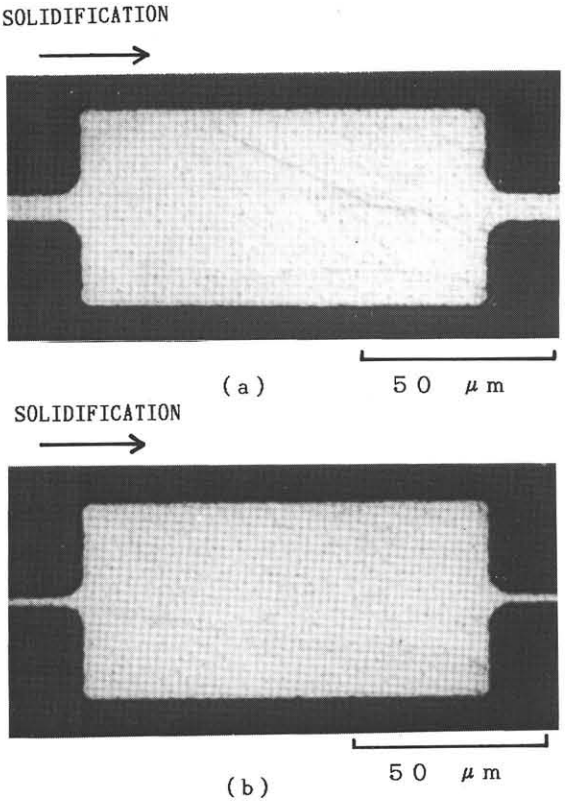


Fig.3 Optical micrographs of an defect-etched silicon surface after recrystallization.

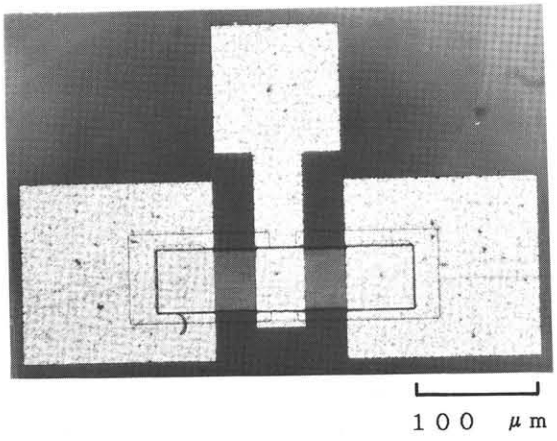


Fig.4 Optical micrograph of a MOSFET fabricated on a recrystallized silicon island.

3. MOSFET characteristics

After the connecting regions were etched down in order to isolate the islands completely, aluminum gate n channel MOSFETs were fabricated on the recrystallized silicon islands. These islands were still called connected islands even after the etching to distinguish them from islands that were isolated before the recrystallization. The same type MOSFETs were also fabricated in isolated silicon islands to investigate the effect of the connecting island.

Figure 4 shows an optical micrograph of a typical MOSFET. The gate width and length of the device were 50 μm and 20 μm, respectively. The thickness of the gate oxide film was 1000 Å.

Figure 5 shows typical I_D-V_G characteristics of devices on a connected, and an isolated, island when the applied voltage (V_D) between source and drain was 5 V. These devices were fabricated using the same processes and had the same dimensions. The leakage current of the device on the connected island was about 10^{-13}A/μm, which was two orders lower than that of the device on the isolated island. This was attributed to, not only a decrease of crystalline defects in the silicon film, but also a decrease of positive charges at the interface between the silicon and the fused silica substrate.

Previous work has already shown that positive charges could be compensated by implanting boron ions at the interface region.[9] Figure 6 shows the leakage current of devices on silicon where boron ions were implanted over the range of 10^{12}-10^{14} cm^{-2}. The abscissa shows the experimental dose value of boron, or the boron concentration at the interface which was calculated using SUPREM simulations. For the isolated island, the leakage current began to decrease at a dose value of 10^{13} cm^{-2}. On the other hand, the leakage current was already below 10^{-13}A/μm at the dose value of 3 x 10^{12} cm^{-2}, for the connected island. It was thought that the positive charge density at the interface corresponded to the boron concentration at the interface when the leakage current began to decrease. The result meant that the positive charge density at the interface was lowered by about one order by recrystallizing the connected island. In the isolated island, silicon was abruptly recrystallized from a supercooled state, so that many dangling silicon bonds and much localized stress probably remained at the interface. On the other hand, in the connected island, silicon was smoothly recrystallized and the number of dangling bonds and the stress were decreased.

Figure 7 shows field effect mobility of the devices at V_D= 0.1 V. The field effect mobility of the connected island was about 900 cm^2/Vs, which was twice that of the isolated island. This was explained as follows. In the (100) orientation of

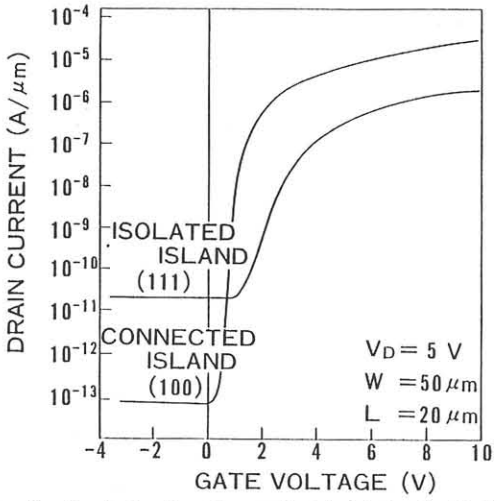


Fig.5 Typical I_D-V_G characteristics of devices fabricated on an isolated, and a connected, island.

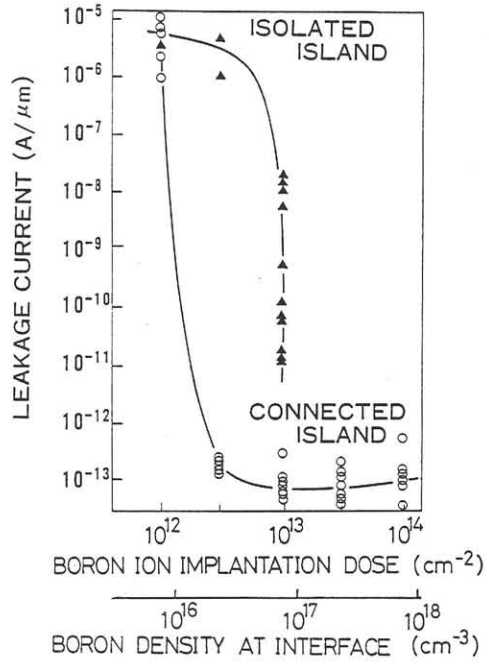


Fig.6 Boron implanted dose dependency of leakage current.

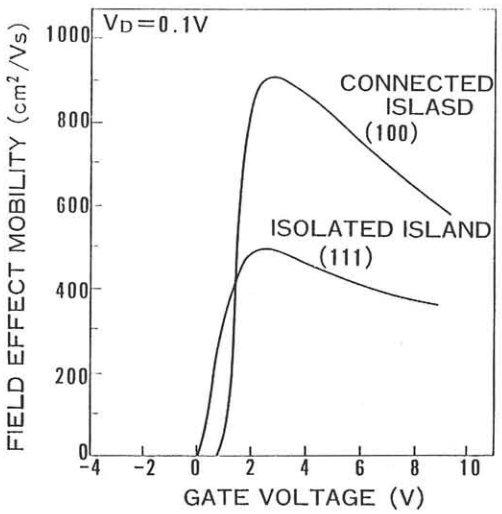
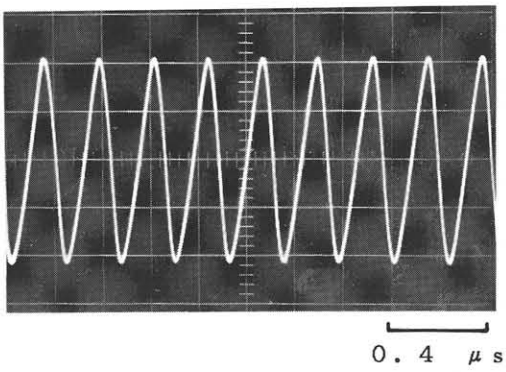


Fig.7 Field effect mobility of devices fabricated on an isolated, and a connected, island.

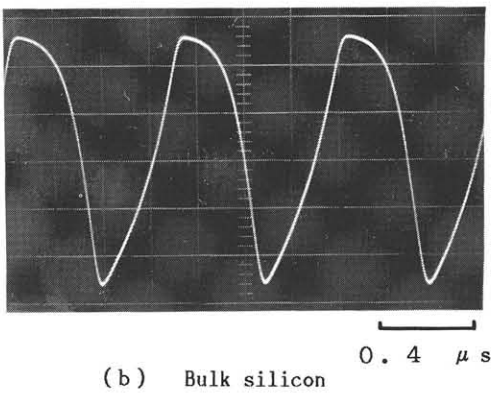
the connected island, the electron mobility was increased by the tensile stress which existed in the silicon layer due to the difference in thermal expansion coefficients between silicon and fused silica substrate.[4,10] On the other hand, in the (111) orientation of the isolated island, the electron mobility was not increased by tensile stress. This was attributed to the difference in shapes of the iso energy planes in the k-spaces between (100) and (111) orientations.[11]

In order to investigate switching speed of MOSFETs fabricated on connected silicon islands, a 51 stage EE MOSFET ring oscillator was fabricated on them. Dimensions of the driver MOSFET (W/L) were 40 μm /10 μm, and those of the load MOSFET (W/L) were 20 μm / 50 μm. The dimension ratio β_R was 10. Thickness of the gate oxide film was 1000 Å. The fabrication process was the same as that of single MOSFET devices.

Figure 8 shows waveforms of the ring oscillator fabricated on the connected islands and that of a ring oscillator fabricated on single crystal bulk silicon. Applied voltage (V_{DD}) was 20 V. Oscillation frequency of the connected island was about 4.5 MHz, and propagation delay time (t_{pd}) was 2.2 ns, which was three times faster than that of bulk silicon. This high speed operation was attributed to a decrease in parastic capacitace.



(a) Recrystallized silicon on fused silica



(b) Bulk silicon

Fig.8 Waveforms of 51 stage EE MOSFET ring oscillators.

4. Summary

The (100) oriented single crystal silicon layer on fused silica could be obtained by recrystallizing connected polycrystalline silicon islands. This decreased the charge density at the silicon - fused silica interface. Consequently, the field effect mobility of the MOSFET fabricated on the connected silicon island was about 900 cm^2/Vs, which was twice that of a MOSFET fabricated on an isolated island. The leakage current of the former was 10^{-13}A/μm, which was two orders lower. Propagation delay time of a EE MOSFET ring oscillator fabricated on the connected island was 2.2 ns, which was three times faster than that of an oscillator on bulk silicon.

Acknowledgments

The authors would like to express their sincere thanks to Dr. T. Takasuna, Dr. F. Nakajima, Dr. Okamura, Mr. K. Miyata, Mr. T. Suzuki and Mr. Y. Hosokawa for their guidance and encouragement.

(References)

1) T. Nishimura, Y. Akasaka, H. Nakata, A. Ishizu and T. Matsumoto ; SID 82 DIGEST, p36, (1982)
2) T.I. Kamins and P.A. Pianetta ; Electron Device Lett., EDL-1, p214, (1980)
3) S.A. Lyon, R.J. Nemanich and D.K. Biegelsen ; Appl. Phys. Lett. 40, p316, (1982)
4) B-Y. Tsaur, John C.C. Fan and M.W. Geis ; Appl. Phys. Lett., 40, p322, (1982)
5) Y. Kobayashi, A. Fukami and T. Suzuki ; Electron Device Lett., EDL-4, p132, (1983)
6) Y. Kobayashi, A. Fukami and T. Suzuki ; Extended Abstracts of 15 th Conference on Solid State Devices nad Materials p35, (1983)
7) Y. Kobayashi, A. Fukami and T. Suzuki ; J. Electrochem. Soc., 131, p1188, (1984)
8) K.A. Bezjian, H.I. Smith and J.M. Carter ; J Electrochem. Soc., 129, p1848, (1982)
9) D. Kranzer, E. Preuss, K. Scholuter and W. Fichtner ; IEEE Trans. Electron Dev., ED-25, p868 (1978)
10) Y. Kobayashi, M. Nakamura and T. Suzuki ; Appl. Phys. Lett., 40, p1040, (1982)
11) C. Herring ; Bell Syst. Tech. J., 34, p237, (1955)