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Vertically Integrated MOS Devices with Double Active Layers

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The integrated MOS device in stacked double active layers is designed and fablicated by using the improved selective laser recrystallization technique and the VLSI technology.

The 15 um wide single crystalline silicon on insulator (SOI) stripes in between straight grain boundaries can be obtained on the already completed MOS devices without any degradation of their electrical characteristics. MOS devices fabricated on this top layer exhibit quite the same electrical characteristics as those of bulk silicon devices, and also the good stability against the potential variation at the underlying device layer.

The performance of the MOS devices in double active layers verifies the designed structure and the technologies used in this work provide the good feasibility of the future three dimensional LSI.

INTRODUCTION

Recently the development of various practical silicon on insulator (SOI) technologies has provided the strong feasibility of the three dimensional (3-D) integration. Several simple structures such as JMOS (1) which was the stacked n- and p-channel MOSFETs with common gate electrode, and the stacked structure (2) consisting of n- and p-channel pair transistors with separate gates and one level of aluminum interconnects have been reported so far. However, the electrical characteristics of MOSFETs on the top layer were still inferior to those of conventional SOI devices (3) and also bulk silicon devices. This is because the recrystallization of polycrystalline silicon (polysilicon) on a complicated device structure is still in poor level as compared with the conventional SOI on a flat insulating substrate.

In this study, the selective laser recrystallization technique (4) was improved and successfully applied for obtaining the single crystalline SOI film supperimposed on already completed MOS devices in bulk silicon without any degradation of their electrical characteristics, and thereby the integrated MOS devices in stacked double active layers were well designed and fabricated.

SELECTIVE LASER RECRYSTALLIZATION

The direct irradiation of laser beam to the underlying layers through the insulating layer should be precluded in order to avoid the destructive damage for the already completed devices.

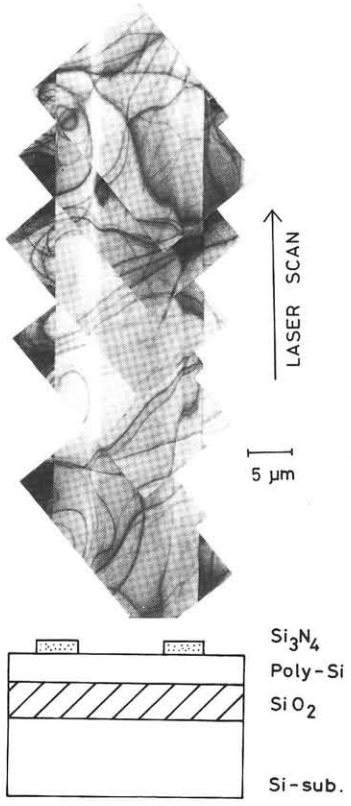


Fig.1 Schematic cross section of the sample structure and a TEM photograph of the recrystallized silicon layer.

Therefore, in this work, the laser recrystallization process was performed without any pattern forming of the polysilicon, but patterned nitride stripes deposited on the polysilicon were used as an antireflecting layer(4) for controlling the thermal profile which was concerned with the location and direction of grain boundaries.

Figure 1 shows the schematic cross section of the basic sample structure and the TEM photograph of the recrystallized silicon layer. The 500-550 A thick chemical vapor deposited Si_3N_4 layer on a 0.5-0.7 um polysilicon film was patterned into parallel stripes of 5 um in width and 10 um in space. The cw argon laser beam of 100 um diameter was rastered parallel to the stripes with a 30 um step for overlapping. Scan speed of 25 cm/sec at substrate temperature of 450 C offered the widest laser power window to allow the grain boundary controlled recrystallization. Although a few stacking faults are contained in the film, TEM photograph shows the 15 um wide single crystalline silicon stripes in between straight grain boundaries can be obtained by this technique.

Figure 2 shows the relation between the laser power for proper recrystallization and the thickness of underlying oxide layer. There was a wide laser power window for various oxide thickness ranging from 0.75 to 1.6 um. This result implies that the corresponding thickness variation is simultaneously applicable in a device structure.

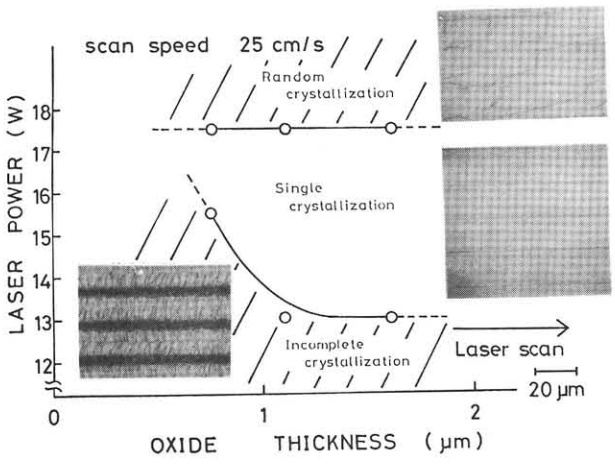


Fig.2 Laser power window for proper recrystallization of polysilicon versus thickness of underlying oxide layer

DESIGN AND FABRICATION

After those preliminary studies, MOS devices in double active layers were designed and fabricated.

The starting material was a 4 inch p-type [100], 20 Ω cm single crystalline silicon wafer. The fabrication steps for NMOS devices on a bottom layer were carried out by a conventional MOS LSI technology. The thickness of the gate oxide and a standard gate length were 400 A and 3 um, respectively. The phosphorus doped polysilicon layer was used as an interconnect layer instead of an aluminum matallization in order to endure the succeeding high temperature processing. After completing the bottom layer processing, a 0.7 um thick LPCVD silicon dioxide(oxide) was deposited, and planarized by a resist coating and the following RIE etching back process. A 0.6 um thick LPCVD oxide was again deposited as an intermediate insulating layer, the total thickness of the thinnest region in the device structure was 0.9 um, which was determined with taking into account of the laser power window. Then 0.5 um LPCVD polysilicon was deposited as a top device layer. After recrystallization, the device region of n- and p- channel MOSFETs were defined with aligning their location to the single crystal region, and ion implanted with total doses of 1×10^{12} P^+/cm^2 and 2×10^{12} B^+/cm^2 by using 2 steps acceleration voltages, respectively. The thickness of the gate oxide measured on the [100] silicon wafer was 650 A. The additional oxide layer was formed on the side wall of the device island to avoid the parasitic transistor. Successive fabrication steps were carried out with a conventional CMOS-LSI process. An aluminum metallization was used as an interconnect layer, and was also connected with the another interconnect layer of the bottom device through contact holes.

The schematic cross section and the SEM view of the finished device configuration are shown in Fig.3.

ELECTRICAL CHARACTERISTICS

The electrical characteristics of MOSFETs fabricated on both top and bottom layers were measured from the devices whose channel regions were vertically aligned each other. Figure 4-(a),(b) and (c) show the typical I-V characteristics of n- and p-channel MOSFETs with L/W = 5/10 (um), on a top layer and n-channel MOSFET on a bottom layer with L/W = 3/10 (um), respectivery.

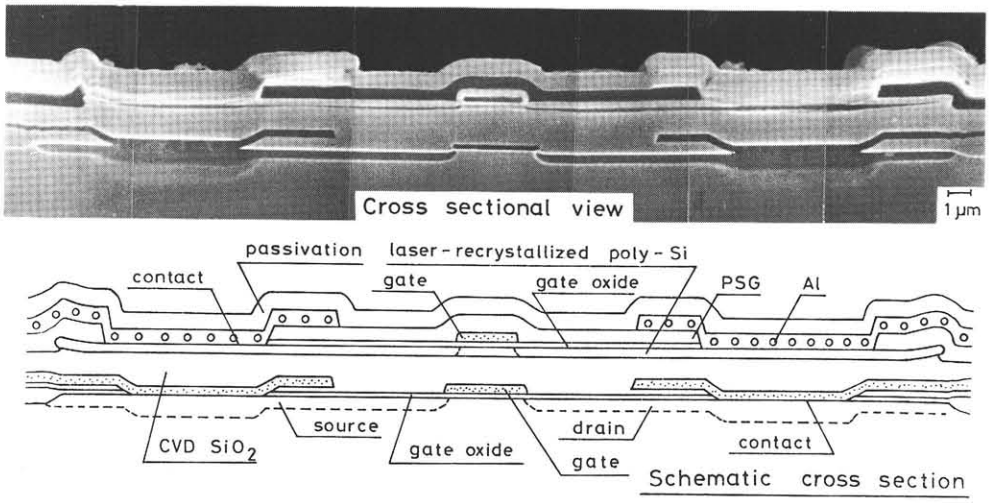


Fig.3 The SEM cross sectional view and the schematic cross section of the vertically stacked MOS devices.

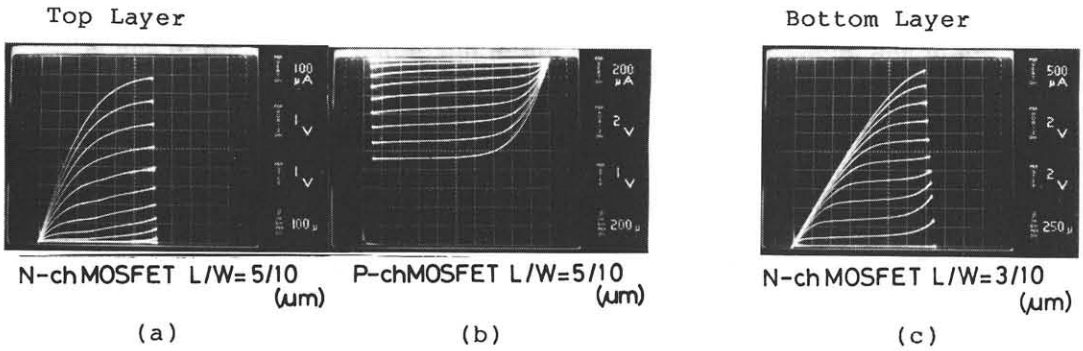


Fig.4 Typical I-V characteristics of MOSFETs fablicated in double active layers.

The surface carrier mobilities obtained from the n- and p-channel MOSFETs both with L/W = 5/10 $(um)_2$ on a top layer were 500 and 230 cm^2/Vsec, respectively. And that of n-channel MOSFETs on a bottom layer was 670 cm^2/Vsec. These results indicated that the crystal quality of the SOI was quite the same with bulk silicon, and the basic characteristics of MOSFETs on a bottom layer was not degraded during the wafer processing. Table 1 summarizes the electrical characteristics of MOSFETs on both top and bottom layers.

Figure 5 shows the subthreshold characteristics of n and p-channel MOSFETs with L/W = 4/10 (um) on a top layer depending on the back gate bias supplied by the interconnect layer of the bottom devices through the thick intermediate layer. Although the subthreshold current of a n-channel device was increased with the back gate bias above 10 V, the leakage current from source to drain was suppressed in very low level below 5 V. In the case of p-channel MOSFETs, nothing but fairly weak dependence of the threshold voltage on the back gate bias voltage was seen. These results indicated that the charge state density at the back surface of the top layer was suppressed in very low level, and therefore the electrical of characteristics of both n- and p-channel MOSFETs were very stable against the potential variation in the underlying device layers.

Table 1 Summary of the electrical characteristics of MOSFETs on both top and bottom layers.

	Bottom Layer	Top Layer	
Material	Bulk-Si	SOI	
Type	NMOS	NMOS	PMOS
L/W(μm)	3/10	5/10	5/10
Vth (V)	0.4	1.5	-2.5
Mobility(cm^2/V·sec)	670	500	230
Subthreshold Characteristics (mV/decade)	85.0	90.0	79.9

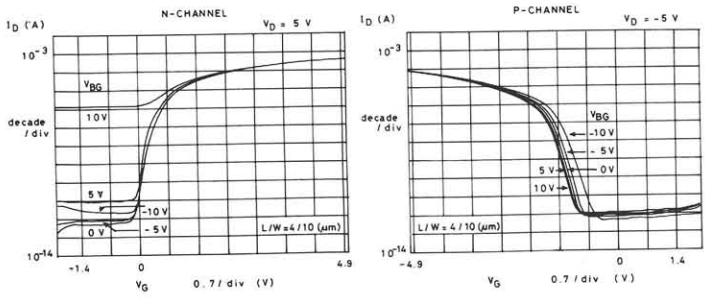


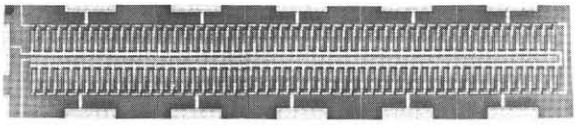
Fig.5 Subthreshold characteristics of MOSFETs on a top layer depending on the back gate voltage supplied from the interconnect layer of the bottom devices through the intermediate insulating layer,

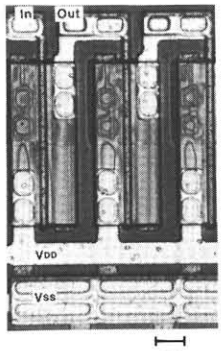
DEVICE

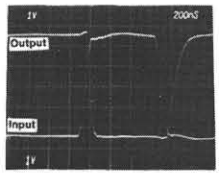
In order to assess the feasibility of 3-D LSI, the inverter was constructed with the combination of a p-channel MOSFET on a top layer and a n-channel MOSFET on a bottom layer, in vertically stacked form and thereby the functional circuit was designed and fabricated.

From the 45 stage CMOS inverter chain shown in Fig.6, the delay time per stage of 2 nsec was obtained at suppy voltage of 5 V.

The CMOS frequency divider shown in Fig.7 operated from the supply voltage of 1.5 V. The maximum operating frequency was 88 MHz at supply voltage above 6 V, and, it was 78 MHz at 5V. These devices were constructed with larger scale integration in double active layered structure than any other devices reported so far (1,2,5), and also exhibited the superior performance to them.

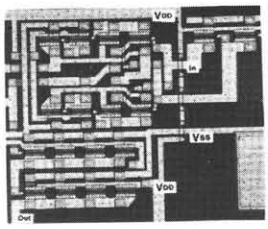






Transfer Characteristic
45 Stages

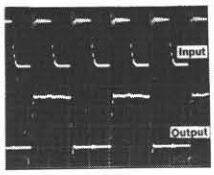
Fig.6 A 45 stage CMOS inverter chain and its typical input-output waveform at supply voltage of 5 V.



1 st Layer NMOS L=3μm
2 nd Layer PMOS L=3μm

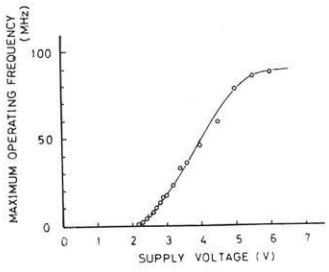
(a)

2 V/div.



In 1 MHz
Out 500 kHz

(b)



(c)

Fig.7 (a) A CMOS frequency divider, (b) Its typical input-output waveform, and (c) The operating characteristics.

CONCLUSION

The integrated MOS devices in stacked double active layers were designed and fabricated by using the improved selective laser recrystallization technique together with the VLSI technology. The device performance verified the superiority of the 3-D structure, and also the designed structure and the technology used in this work offering the good feasibility for the realization of the future 3-D LSI.

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