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# Amorphous Silicon MOSFET's by Anodic Oxidation

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The anodic oxidation in AGW electrolyte is applied to Al/a-Si:H structures to form $Al_2O_3$/native oxide/a-Si:H gate structure. Interface properties of this MOS structure as well as fabrication of a-Si:H MOSFETs are investigated. Resulting FETs show maximum effective mobility of 0.2 $cm^2/Vs$ after proper low temperature annealing in $H_2$. The feasibility of a planar a-Si integrated circuits is demonstrated by fabricating integrated image sensors.

## 1. Introduction

Anodic oxidation allows formation of uniform thin and thick $SiO_2$ and $Al_2O_3/SiO_2$ insulating layers on hydrogenated amorphous silicon (a-Si:H) films at room temperature[1]. The anodic oxidation process is shown to be stable, reproducible and electrically controlable as shown in ref.1. The purpose of the present paper is to describe a-Si:H planar MOSFETs fabricated by such a process. Details of oxidation process, MOS interface study, fabrication process and performance of MOSFETs, especially MOSFETs with $Al_2O_3/SiO_2$ double layer gate insulator, are presented. The double layer gate insulator is expected to reduce the interface state density and improve a-Si:H MOSFET characteristics since the interface consists of native oxide/a-Si:H. The results seem to open up the possibility of a-Si:H MOS integrated circuits with rich functional capabilities.

## 2. Formation and Interface Study of $Al_2O_3$/native $SiO_2$/a-Si:H MOS Structure

### 2.1 Formation of $Al_2O_3$/native $SiO_2$ Double Insulating Films

a-Si:H films to be anodized were prepared by glow-discharge decomposition of $SiH_4$ + $H_2$ gas mixture ($SiH_4$:11%) at gas pressure of 2-3 Torr with gas flow rate of 50 SCCM onto $n^+$ crystalline silicon substrates. The substrate temperature of 270°C was used and the input RF power (13.56 MHz) during deposition was 20-25W.

$Al_2O_3$/native $SiO_2$ double insulating layer was formed either by oxidizing Al/a-Si:H structure or by oxidizing Al in Al/$SiO_2$/a-Si:H structure in which native oxide was formed prior to Al deposition by anodic oxidation. Al was deposited in vacuum onto the grown a-Si:H film at substrate temperature range of 80-150 °C. The anodic oxidation set-up is shown in Fig.1. The electrolyte for anodization is AGW electrolyte[2], which is a mixture of 3% aqueous solution of tartaric acid and propylene glycol. The anodization was done in constant current mode.

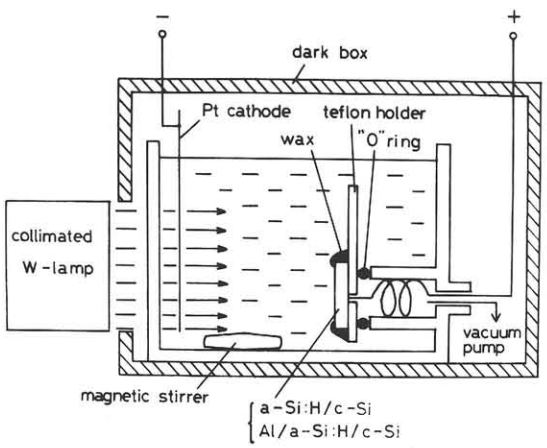



Figure 1 Anodic oxidation set-up

Since holes are required for anodization of a-Si:H, the anode was illuminated by W-lamp (70000 lx) during anodization. Resulting $Al_2O_3$ and $SiO_2$ thickness were 1200Å and 60Å, respectively. Figure 2 (a) and (b) shows the cell voltage change versus anodization time during oxidation of a-Si:H and Al/a-Si:H structures. It was easy to detect the end of Al oxidation in oxidation of Al/a-Si:H structure, since the slope in cell voltage versus oxidation time curve changes at the point of transition from Al oxidation to a-Si:H oxidation.

Table 1 shows the parameters of the anodic oxidation together with the electrical characteristics of anodic oxide films. Resistivity and breakdown field strength of $Al_2O_3$/native $SiO_2$ double layer structures are adequate for an FET gate insulator.

After anodization, Al was evaporated as gate electrodes of MOS diodes, which were used for the study of the MOS interface.

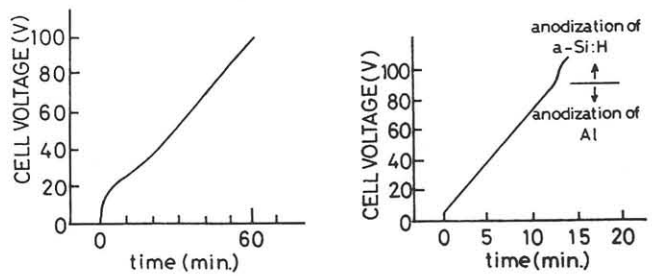
### 2.2 Interface Study of $Al_2O_3$/native $SiO_2$/a-Si:H MOS Structure

MOS structures allow standard C-V and DLTS measurement for interface state and bulk deep trap measurements. G-V characteristics in MOSFET structures may also be used to provide useful information concerning the interface states.

Figure 3 shows low frequency (5 Hz) MOS C-V characteristics of double layer insulator with native oxide grown prior to the $Al_2O_3$ formation. Two structures are present in the C-V curve. The one on the positive bias side is believed to indicate the movement of surface potential in the energy gap by applying the external bias voltage. The other one on the negative bias side is probably caused by the long time constant of the states well under the conduction band. As the surface Fermi level moves away from the conduction band by increasing the negative bias, the states well under conduction band having long time constant can no longer respond to the measurement frequency, thus capacitance of the MOS diode becoming the series capacitance of oxide capacitance and the depletion layer capacitance.

C-V curve shown in Fig. 3 is used to calculate the effective gapstate density including contribution both from the gapstates and from the interface states. The effective gapstate density distribution calculated from Fig. 3 is shown in Fig. 4. Although it was not possible to determine the surface potential with respect to the conduction band, Fig. 4 shows that the surface potential can be moved for more than 1 eV using the double layer structure.

Figure 5 shows MOS C-V data of $Al_2O_3$/native $SiO_2$/a-Si:H structure at room temperature. Increasing annealing temperature, the capacitance of the MOS diode starts to show an increase at higher frequency than that of as-grown samples. On




(a) a-Si:H (b) Al/a-Si:H structure

Figure 2 Cell voltage change vs. time during anodization

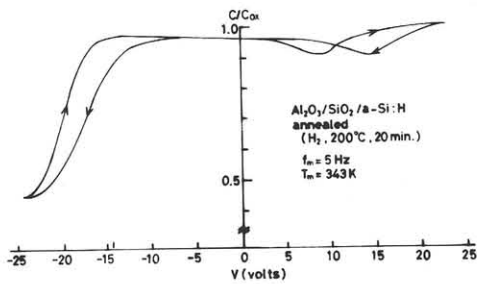



Figure 3 MOS C-V data of $Al_2O_3$/native $SiO_2$/a-Si:H structure at 70 °C. The measurement frequency was 5 Hz. The native oxide was grown prior to the growth of $Al_2O_3$.

Table.1 Parameters of anodization and the electrical properties of anodic oxide films

| material | voltage growth rate (Å/V) | formation rate ($cm^3$/coul.) | material | resistivity (ohms.cm) | breakdown field strength (V/cm) |
|---|---|---|---|---|---|
| a-Si:H | 5.5 | $4.6 \times 10^{-7}$ | $SiO_2$ | $10^{12}$ | $1 \times 10^7$ |
| Al/a-Si:H | 13.5 | $5 \times 10^{-5}$ | $Al_2O_3/SiO_2$ | $10^{15}$ | $3 \times 10^6$ |

the basis of the interpretation of C-V curve presented above, this result indicates that the effective gapstate density is reduced by the annealing. It is believed that the improvement in C-V curves are mainly caused by the reduction of the interface states and not by the reduction of the gapstates, since the annealing temperatures are well below the substrate temperature during deposition of a-Si:H.

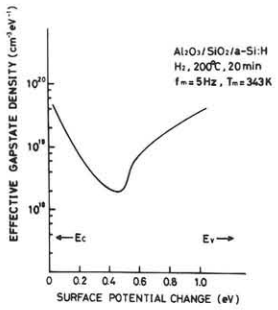



Figure4

Effective gapstate density distribution in $Al_2O_3/SiO_2$ /a-Si:H structure calculated from Fig. 3.

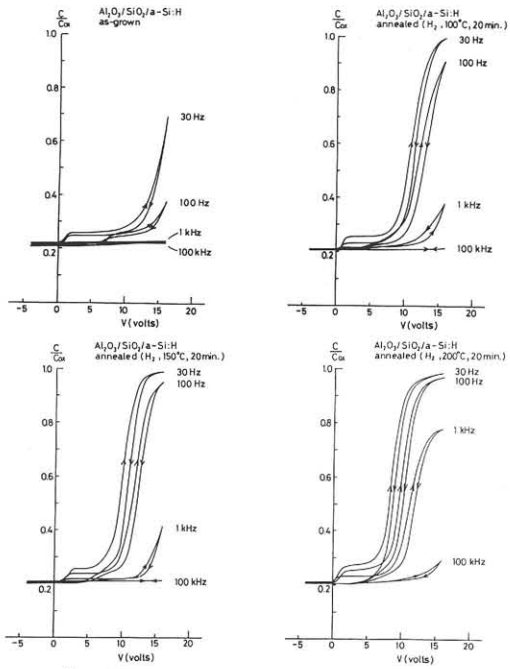



Figure 5 MOS C-V characteristics at room temperature. The structure was formed by the oxidation of Al/a-Si:H.

## 3. Characteristics of a-Si:H MOSFETs

### 3.1 Fabrication Processes of a-Si:H MOSFETs

Outline of the fabrication process of a-Si:H MOSFETs is summarized in Fig.6. This process allows fabrication of fully planar MOSFETs. a-Si:H films were deposited on the glass (Corning 7059) by RF glow discharge decomposition of $SiH_4$ under the same conditions of MOS diode fabrication (section 2.1.). Phosphine gas was added in $SiH_4$ to obtain $n^+$-layer, which was used to make ohmic contacts between source/drain electrodes and the a-Si:H film. The $n^+$-layer on the channel and device separation region was chemically etched off using an etchant consist of $HF:HNO_3:CH_3COOH$ = 3:5:15, which has etching rate of 0.3 μm/min for a-Si:H.

$Al_2O_3$/native $SiO_2$ double insulating layer was grown by anodization of an Al/a-Si:H structure. The conditions of Al deposition and anodic oxidation are the same for the MOS diode fabrication. After a-Si:H MOSFET fabrication, annealing in $H_2$ gas at temperature range of 160-230 °C was done to improve the FET characteristics.

Figure 7 shows a cross sectional view of the fabricated FET. The gate length and the gate width of the fabricated FET were 110μm and 3.9mm, respectively. The gate width was designed to be adequately wide in order to obtain a reasonable drain current level, which is typical for a-Si:H FETs due to the low conductivity of the material.

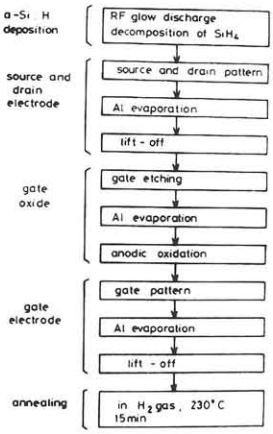



Figure 6

Outline of the fabrication process of a-Si:H MOSFETs

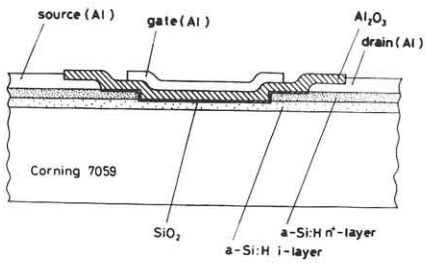



Figure 7 Cross sectional view of a-Si:H MOSFET

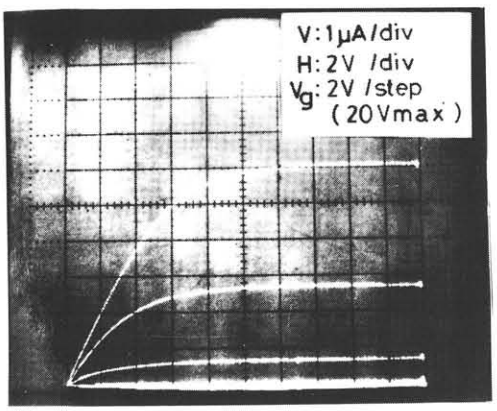



Figure 8

Drain current versus drain voltage characteristics of an a-Si:H MOSFET

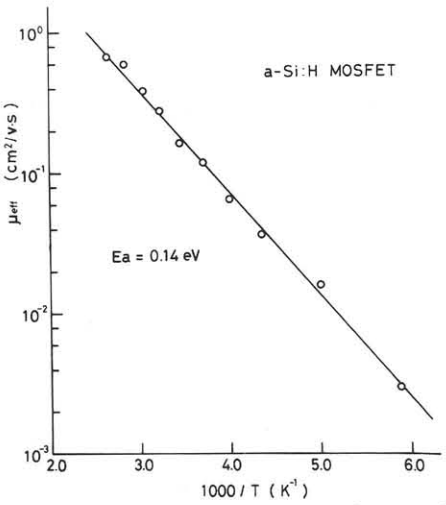



Figure 9 Temperature dependence of effective mobility

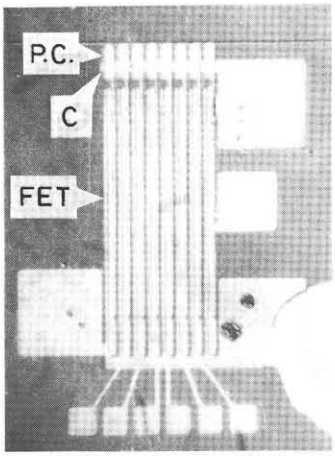



Figure 10 a-Si:H integrated image sensor

### 3.2 Characteristics of a-Si:H MOSFET

Figure 8 shows the drain current $I_d$ versus drain voltage $V_{ds}$ characteristics of the fabricated a-Si:H MOSFET after annealing. The annealing was done in $H_2$ gas at 230℃ for 15min. The highest effective mobility $\mu_{eff}$, calculated from $\mu_{eff} = (L/W)(1/C_{ox})\ (I_d/V_g)(1/V_{ds})$, was 0.2 $cm^2/Vs$. The annealing process greatly enhanced the effective mobility by a factor of 2-10, which was typically 0.002-0.05 $cm^2/Vs$ prior to annealing. It is believed that this improvement is due to the reduction of interface state densities at insulator/a-Si:H interface by annealing as shown in Fig.5. Figure 9 shows the temperature dependence of the effective mobility. The effective mobility increased with temperature with an activation energy of 0.14 eV, indicating trap controlled non-dispersive transport. The mobility value at the high temperature limit was as high as 60 $cm^2/Vs$.

In order to show the feasibility of the planar a-Si integrated circuits by the present technology, an 8-bit one-dimensional integrated image sensor shown in Fig.10 was fabricated. a-Si:H integrated image sensor consists of photodetectors, MOSFETs and charge storage capacitors. These basic devices were separately fabricated at first to clarify the characteristics of each device.

An interdigital planar photoconductor and a MOS photodiode were investigated for the detector of the image sensor. In both cases, MOS films were found useful either for surface passivation/anti-reflection films or for enhancement of diode breakdown voltage. The response speed of the photoconductor was a few hundred usec, whereas that of the MOS photodiode was very high, being 70 ns for a load resistance of 5 ohms. Charge storage capacitors were formed by anodizing Al films as well. Anodization allows formation of high-quality barrier-type $Al_2O_3$ films. This a-Si:H integrated image sensor should allow a cycle time of 100 μsec.

### 4. Conclusions

The anodic oxidation in AGW electrolyte was used to form $Al_2O_3$/native oxide/a-Si:H gate structure for a-Si:H MOSFETs. Resulting FETs showed maximum effective mobility of 0.2 $cm^2/Vs$ after proper low temperature annealing. MOS interface study showed that this improvement is possibly due to the reduction of interface state density by annealing in $H_2$. The results seem to open up the possibility of a-Si:H MOS integrated circuits with rich functional capabilities.

### Acknowledements

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### References

1) H. Yamamoto, S. Arimoto, H. Hasegawa, H. Ohno and J. Nanjo : Electron. Lett. 19(1983)6

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