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High Transconductance Si-TFT's Using Ta_2O_5 Films as Gate Insulators

Shunji Seki, Takashi Unagami and Bunjiro Tsujiyama

Ibaraki Electrical Communication Laboratory
Nippon Telegraph and Telephone Public Corporation

Tokai, Ibaraki 319-11, Japan

p-channel thin-film transistors (TFTs) have been fabricated in layers of laser-recrystallized polycrystalline silcon on fused quartz substrates using magnetron-sputtered tantalum pentoxide (Ta_2O_5) as a gate insulator. These TFTs have exhibited p-channel enhancement mode characteristics with a threshold voltage of -0.1 V, a transconductance of 150 μS at Vg = -5 V and a breakdown voltage exceeding 100 V. An on-off current ratio exceeding 10^4 has been obtained. The fundamental circuit consisting of these TFTs and a storage capacitor using Ta_2O_5 as its dielectric material have indicated enough switching characteristics for thin-film electroluminescent (TFEL) displays.

1. Introduction

In recent years, thin-film transistors (TFTs) with their active channels in layers of laser-recrystallized polycrystalline silicon on transparent glass substrates have attracted much attention, offering interesting applications in large-area, flat panel displays.[1,2] For addressing thin-film electroluminescent (TFEL) displays, offset gate structure Si-TFTs with high breakdown voltage have been designed and fabricated on quartz.[2] However, these Si-TFTs have exhibited a low transconductance. Due to the necessity of relatively high currents for TFEL displays, geometrical size of these Si-TFTs has become large, which has restrained the resolution and integration of TFEL displays. Furthermore, these Si-TFTs have shown a relatively high threshold voltage, which has prevented lowering the addressing voltage of TFT-TFEL displays.

In order to obtain high breakdown voltage Si-TFTs with a high transconductance and low threshold voltage, it has become increasingly important to explore a higher dielectric constant gate insulator, in addition to obtaining high quality silicon layers on insulating substrates. The authors have investigated electrical properties of high dielectric constant Ta_2O_5 films,[3] electrical properties at the Ta_2O_5/Si interface,[4] and an appropriate dry etching technique for deposited Ta_2O_5[5] for its application to a gate insulator for Si-TFTs.

This paper reports the fabrication of offset gate structure Si-TFTs employing rf-magnetron sputtered Ta_2O_5 films as gate insulators on fused quartz substrates for addressing TFEL displays.

2. Device Fabrication

The schematic of the device fabrication processing sequence is depicted in Fig.1. Fused quartz substrates obtained in the shape of three-inch diameter discs about 380 μm thick were used to be compatible with the conventional silicon device fabrication steps. A 500 nm thick layer of LPCVD polycrystalline silicon was deposited at 625°C. The polycrystalline silicon layer was encapsulated by a 170 nm thick layer of CVD silicon dioxide and was then recrystallized by a scanning CW Ar laser in a dry nytrogen flow. The substrates were maintained at 400°C during the recrystallization. The laser power was adjusted to 8.2 W. After laser annealing, the encapsulation layers were etched away, and the silicon islands, upon which the transistors would be fabricated, were formed using CF_4 plasma etching. A 100 nm thick Ta_2O_5 gate insulator (ε = 20, breakdown voltage = 4 to 5×10^6 V/cm) was deposited at room temperature by an rf-magnetron

sputtering system. The sputtering gas consisted of a mixture of argon and oxygen. Following the Ta_2O_5 deposition, the substrates were masked with photoresist and etched by the reactive ion etching (RIE) using CF_4 as a reactive gas. Finally, Al was electron-beam evaporated and patterned for the contacts. Prior to measurements, the devices were annealed in a mixture of hydrogen and nitrogen at 450°C for 30 minutes.

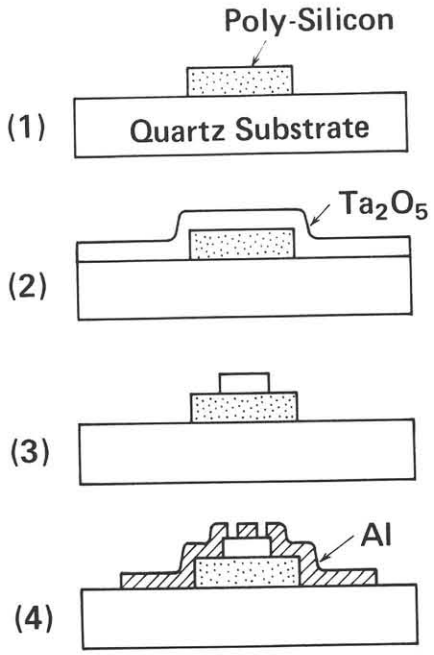

Fig. 1 Schematic of the device fabrication processing sequence.
(1) LPCVD poly-Si deposition, laser annealing and poly-Si islands formation.
(2) Ta_2O_5 gate insulator deposition.
(3) Patterning for Ta_2O_5 using RIE.
(4) Al metallization.

3. Device Characteristics

The typical drain-source I-V characteristics are shown in Fig.2. The channel length, the channel width and the offset gate length are 10 μm, 100 μm and 7 μm, respectively. Well-saturated drain-source characteristics have been obtained. The device exhibits p-channel enhancement mode characteristics. The threshold voltage is -0.1 V and the transconductance is 150 μS at gate bias voltage V_g = -5 V. In p-channel TFTs employing SiO_2 as a gate insulator, the large enhancement threshold voltage was observed due to the large positive fixed charge density at the SiO_2/Si interface.[6] It is useful to employ Ta_2O_5 as a gate insulator in reducing the threshold voltage because of the negative charge density ranging from -1 to -3×10^{11} cm^{-2} at the Ta_2O_5/Si interface.[4]

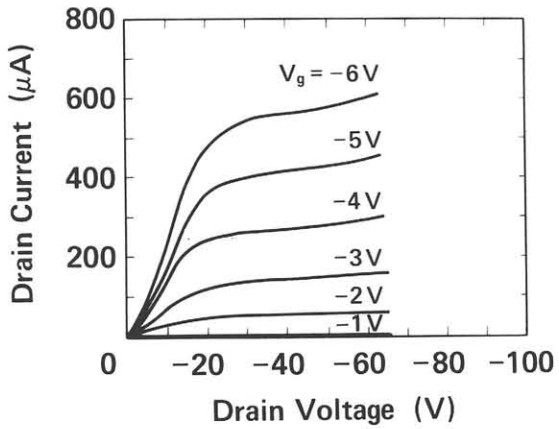

Fig. 2 Drain-source I-V characterisitics. The channel length, the channel width and the offset gate length are 10 μm, 100 μm and 7 μm, respectively.

Figure 3 shows the dependence of the drain-source current on the gate bias voltage. The leakage current was measured to be 5.3×10^{-10} A/μm (per unit channel width) at drain-source voltage V_d = -50 V and gate bias voltage V_g = 1 V (off state). The on-off current ratio of more than 10^4 has been obtained for gate bias voltage variation from 1 V to -5 V, which is sufficient for the swithcing matrix element of TFEL displays.

Offset gate structure TFTs have the advantage of obtaining high drain breakdown voltage.[2] In the device shown in Fig.2, the breakdown voltage was measured to be over 100 V. Figure 4 shows the dependence of the breakdown voltage on the offset gate length. Offset gate length was varied in the range from 7 μm to 16.8 μm. Breakdown voltage tends to increase with the offset gate length. As shown in Fig.4, the breakdown voltage exceeding 200 V was observed for the device with the offset gate length of 16.8 μm. The threshold voltages were in the range from 0 V to -1 V, independent of the offset gate length. These characteristics have indicated that these Si-TFTs using rf-magnetron sputtered Ta_2O_5 as a gate insulator have

sufficient capability of addressing TFEL displays. In addition, due to the high transconductance of these Si-TFTs, it becomes possible to reduce their geometrical size in their application to TFT-TFEL displays.

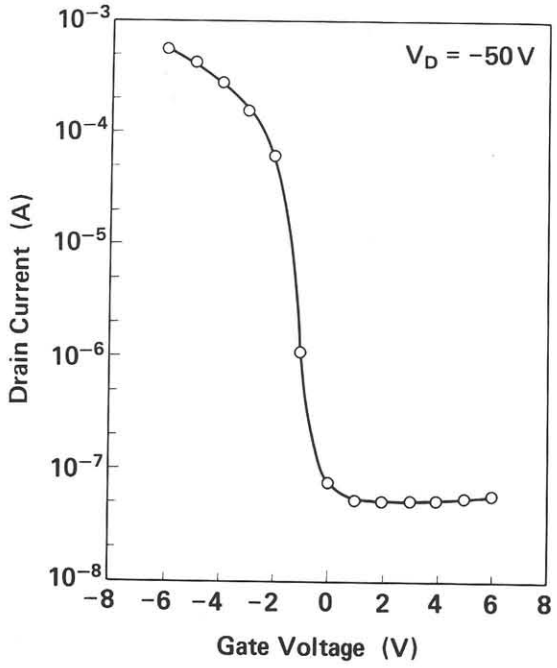

Fig. 3 The dependence of the drain current on the gate bias voltage. The channel length, the channel width and the offset gate length are 10 μm, 100 μm and 7 μm, respectively.

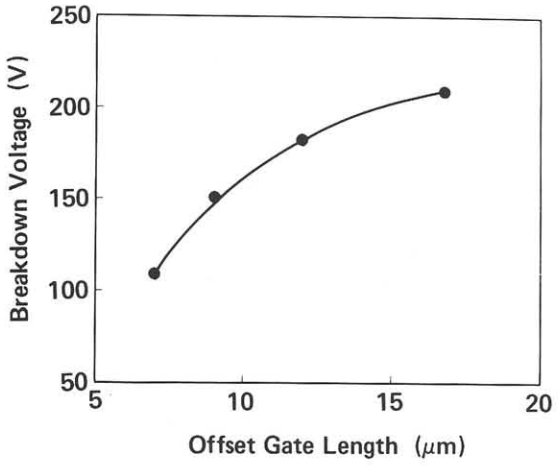

Fig. 4 The dependence of the breakdown voltage on the offset gate length. The channel lengh and the channel width are 10 μm and 100 μm.

4. TFT-circuit

The fundamental circuit was fabricated using these high transconductance Si-TFTs. The fabricated circuit is shown in Fig.5. This is an elemental circuit of each picture element in the active matrix for TFEL displays, and it consists of two TFTs and one capacitor. Due to the necessity of the high breakdown voltage in the off state and relatively high currents in the on state, high breakdown voltage TFTs with high transconductance are required. The capacitor C_s acts as a storage capacitor, which allows the TFEL display to be driven with a 100% duty factor.

The channel length, the channel width and the offset gate length of TFT-1 and TFT-2 are 10 μm, 100 μm and 7.5 μm, respectivley. The Ta_2O_5 gate insulator thickness is 100 nm for both TFTs. Magnetron-sputtered Ta_2O_5 was also used as a dielectric material of this storage capacitor. Its electrode area is 100 μm x 100 μm and the Ta_2O_5 thickness is 100 nm.

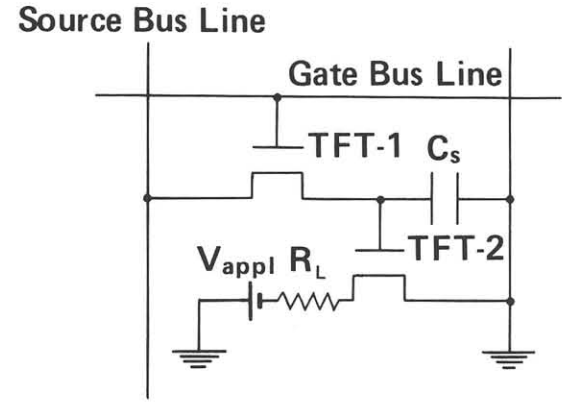

Fig. 5 TFT-circuit. The channel length, the channel width and the offset gate length of TFT-1 and TFT-2 are 10 μm, 100 μm and 7.5 μm, respectively. The storage capacitor C_s is 100-nm thick Ta_2O_5 with the area of 100 μm x 100 μm.

This TFT-circuit was fabricated as follows: (1) Ta_2O_5 deposition for a storage capacitor by rf-magnetorn sputtering onto the substrates on which TFT-1 and TFT-2 had been fabricated. (2) Patterning for Ta_2O_5 using RIE. (3) Al metallization and patterning for the contacts. (4) Annealing in a mixture of hydrogen and nitrogen at 450°C for 30 minutes.

In order to evaluate the capability of this circuit, the output characteristics were simulated using 10-MΩ resistance as a load. The output characterisitcs are shown in Fig.6. The gate bus voltage of -5 V was applied to turn on the TFT-1. Under this condition, the source bus voltage could be applied to the gate electrode of the TFT-2. As shown in Fig.6, the applied voltages were varied from 50 V to 100 V, which was commonly used to drive TFEL displays. The output voltage measured at the load resistance could be controlled by varying the source bus voltage. The output voltage was changed from 35 V to 95 V by varying the source bus voltage from 0 V to -5 V, when the applied voltage was 100 V. These characteristics have shown that this circuit have enough potential for addressing TFEL displays.

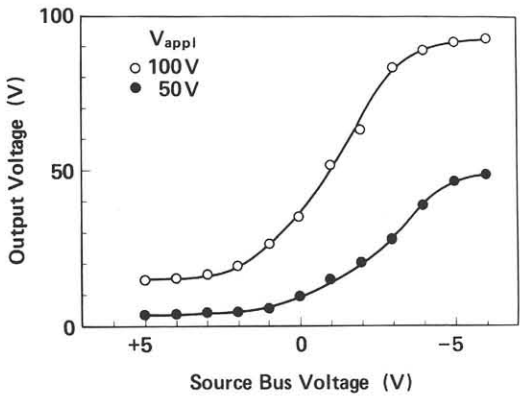

Fig. 6 The output characteristics as a function of the source bus voltage. The load resistance is 10 MΩ and the gate bus voltage is -5 V.

5. Conclusions

High breakdown voltage Si-TFTs with a high transconductance and low threshold voltage have been fabricated in laser-recrystallized polycrystalline silicon on quartz substrates by employing magnetron-sputtered Ta_2O_5 as a gate insulator. These TFTs with 7-μm offset gate length have exhibited p-channel enhancement mode characteristics with the threshold voltage of -0.1 V and the transconductance of 150 μS at V_g = -5 V. The leakage current has been measured to be 5.3×10^{-10} A/μm (per unit channel width). The sufficient on-off current ratio exceeding 10^4 and drain-source breakdown voltage of more than 100 V have been obtained. The fundamental circuit consisting of two TFTs and one storage capacitor have indicated enough switching characteristics: the output voltage can be changed from 35 V to 95 V by varying the source bus voltage from 0 V to -5 V, when the applied voltage is 100 V. These characteristics have indicated that Si-TFTs using rf-magnetron sputtered Ta_2O_5 as a gate insulator have the sufficient capability of addressing TFEL displays. Furthermore, due to their high transconductance by employing Ta_2O_5 gate insulator, it has become possible to reduce the geometrical size of these TFTs, which enables to increase the resolution and integration of TFEL displays.

6. References

(1) T.I.Kamins and P.A.Pianetta, IEEE Electron Device Lett., EDL-1, 214 (1980).
(2) T.Unagami and B.Tsujiyama, IEEE Electron Device Lett., EDL-3, 167 (1982).
(3) S.Seki, T.Unagami and B.Tsujiyama, J. Vac. Sci. Technol. A, 1, 1825 (1983).
(4) S.Seki, T.Unagami and B.Tsujiyama, J. Electrochem. Soc., to be published.
(5) S.Seki, T.Unagami and B.Tsujiyama, J. Electrochem. Soc., 130, 2505 (1983).
(6) S.D.Malhi, P.K.Chatterjee, R.F.Pinizzotto, H.W.Lam, C.E.C.Chen, H.Shichijo, R.R.Shah and D.W.Vellavance, IEEE Electron Device Lett., EDL-4, 369 (1983).