Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 77-81



**Invited**

# Very Short Channel MOSFET's-Physics and Technology

*W. Fichtner*

AT&T Bell Laboratories
Murray Hill, New Jersey 07974

*ABSTRACT*

This paper reviews recent work in the area of scaled MOSFET device structures. It summarizes the major aspects of device scaling and it illustrates the strong coupling between device performance and device fabrication. Devices with channel lengths below 0.25$\mu m$ have been fabricated using advanced pattern transfer techniques and minimum heat treatment cycles. Experimental results demonstrate the scaling properties of these devices.

## I. Introduction

The increase in complexity in silicon integrated circuits has been mainly achieved by reducing the dimensions of the most important building blocks of a chip, the MOSFET. Further progress in VLSI will certainly push MOSFET dimensions to 0.5$\mu$m or less.

This paper summarizes recent results in the field of MOSFET scaling and submicron device technology. It includes some results on the electrical performance of very small n- and p-channel devices.

## II. Device Physics, Scaling Considerations and Hot-Carrier Effects

### 1. MOSFET Scaling

The reduction of the dimensions of the active device forces a tradeoff between various variables, such as the channel length, channel doping, oxide thickness, junction depth and the supply voltage. Figure 1 shows the minimum channel length for which long channel behavior can be observed as a function of these parameters. This empirical relationship has been obtained from a large series of experiments and numerical simulations for channel lengths ranging from 20$\mu$m to 0.25$\mu$m [1]. The inset in the figure defines MOSFET parameters. Compared to other scaling rules, such as constant-field and constant-voltage scaling, the dependence of the minimum channel length $L_{\min}$ on $\gamma$ offers enhanced flexibility and better tradeoff.

The performance of small devices depends critically on the gate oxide. For devices with 1$\mu$m gatelength and smaller, very thin oxides ($d < 250$Å) are required. The reduction of gate oxide thickness is limited by various physical phenomena, such as tunneling, the Poole-Frenkel effect and breakdown.

The doping level in the channel region is determined by the maximum supply voltage and the threshold voltage. For a submicron device, this doping level is close to $10^{17}$cm$^{-3}$, which is high enough to prevent punch-through effects.

The most critical hurdle to overcome in the scaling of MOS devices arises from hot-carrier effects. The basic operation of the MOSFET in the saturation regime results in a reverse biased junction between the channel region and the drain junction region. This junction can break down at relatively low voltages, forcing a reduction of the bias supply.

### 2. Hot Carrier Effects

Figure 2 shows the distribution of the lateral electric field for an enhancement mode MOSFET with a gatelength of 1$\mu$m biased at $V_{gs} = 1$V, $V_{ds} = 3$V. Near the source contact, the field is negative due to the diffusion barrier between the highly doped source region and the channel. The field gradually increases until it reaches a maximum close to the drain contact. From the picture, one can recognize the strong nonuniformity of the field along the channel. Furthermore, it is evident from the magnitude of the field near the drain that impact ionization is a problem in small planar MOSFET structures. In Fig. 2, the maximum field value is $2.8\times10^5$ V cm$^{-1}$, clearly high enough to cause impact ionization.

The influence of the high electric fields in small MOSFETS can seriously degrade their performance due to the generation of gate and substrate currents. For submicron-size dimensions, the high-field behavior differs drastically for n- and p-channel devices.

a. In n-channel devices, electrons gain energy as they travel along the channel. Some *lucky electrons* may gain enough energy and surmount the Si–$SiO_2$ barrier. Some of these electrons will be trapped in the oxide while others will traverse the oxide and contribute to an effective gate current. Trapping of electrons generates a negative oxide charge ( and no interface traps )[2], therefore resulting in a decrease of current.

   In the saturation region, $V_{ds} > V_{gs}$, which results in a reversal of the normal electric field near the drain and forces the carriers into the bulk. The high electric field in this region generates electron-hole pairs. While generated electrons are forced into the drain junction area, thus augmenting the drain current, the generated holes travel backwards to the interface where they are deflected into the substrate, contributing to the substrate current. It is very unlikely for holes to surmount the oxide barrier.

b. In the case of p-channel devices, lucky holes are very unlikely. However, contrary to the n-channel situation just described, generated electrons travelling back towards the interface *can* overcome the oxide barrier. It is important to note that in p-channel devices, a hot-hole current or hot-hole trapping have not been observed [2]. There is a hot-electron gate current, however, which is due to drain avalanche. This gate current peaks at low gate voltages corresponding to the maxima of the substrate current. Trapping effects can occur in p-channel devices, resulting in an increase of channel current.

Since ionization rates of electrons are much larger than corresponding hole values, major emphasis has to be given to the optimization of the n-channel transistors. While gate currents are comparable for similar gate voltages, the substrate currents in n-channel devices are typically four to five orders of magnitude larger than corresponding p-channel results.

Figure 3 shows experimental substrate currents as a function of $V_{gs}$ for a small n-channel device. This result is typical for submicron size devices. In order to reduce the substrate current to values below 10 nA $\mu m^{-1}$, the drain voltage would have to be reduced to 2 V.

### III. Technology Considerations

The successful fabrication of devices with submicron features puts stringent requirements on the technology. In the following, recent results are presented to illustrate several important aspects.

#### 1. Pattern Definition and Transfer

Optical lithography has traditionally dominated the pattern definition process. Today's step-and-repeat machines are capable to define minimum feature sizes of slightly under 1$\mu$m with realignment better than 0.25$\mu$m. Figure 4 shows a SEM micrograph of the metal level of a digital IC [3] designed in 1$\mu$m NMOS technology [4]. One should note the excellent uniformity of the metal patterns and the good alignment as exemplified by the contact holes.

For submicron size features, optical lithography becomes increasingly difficult to apply due to problems associated with diffraction, depth-of-field, the size of the exposure field, etc. While encouraging progress has been made, which eventually will lead to optical lithography at 0.5$\mu$m [5], only X-ray [6] and e-beam lithography [7] offer the ultimate capabilities for even smaller patterns. At this point in time, the direct exposure using e-beams fulfills all necessary requirements for submicron feature definition, including linewidth control, registration and overlay accuracy and reproducibility. A typical example showing the capabilities of e-beam lithography in given in Fig. 5. The figure shows the polysilicon level of a part of a digital circuit with 0.5$\mu$m design rules. This pattern has been defined in trilevel resist, and has been transferred using dry etching techniques.

#### 2. Low Temperature Processing

The successful fabrication of submicron device structures can only be successful if the heat cycles of the process are kept as short as possible and at the lowest temperature [8]. The most critical temperature steps in a MOS process include the gate oxide growth step and the heat cycles following the source-drain implants. For devices with channel lengths below 0.5$\mu$m, the gate oxide must be thinner than 150Å. In order to control the growth of this oxide, and to avoid excessive segregation and dopant redistribution, temperatures have to be kept below 900°C.

The performance of small devices is strongly dependent on the structure and the shape of the source-drain areas. Devices with gate lengths of 0.5$\mu$m or smaller must have junctions depths of 0.1 to 0.15$\mu$m. This requirement puts an upper limit on the maximum heat cycle possible. However, the doping in the source-drain areas should be as high as possible to ensure a proper contact formation and to reduce parasitic resistive components.

For n-channel devices, very shallow junctions can be formed. Figure 6 shows a TEM micrograph of the gate-junction area of a scaled MOSFET [9] and a simulated arsenic depth profile in the junction area. The total heat treatment after source-drain implantation was limited to a total of 20 min at 900°C. This heat cycle was established from earlier, more extensive diffusion and annealing studies of As in Si [10].

Compared to n-channel devices, the formation of shallow junctions is much more critical for p-channel devices. Because of its high solubility in Si, B is the preferred doping species as compared to Al and Ga. The high diffusivity of B renders it necessary to keep heat treatments at temperatures not higher than 900°C and as short as possible. An additional problem is the range of implanted B which is much larger than corresponding values for As.

One important consideration in the choice of a proper anneal cycle lies in the regrowth and recrystallization properties of the as-implanted regions. During the implantation process, silicon interstitials and the implanted atoms, which are also at interstitial locations, form clusters and/or precipitates. The formation of an amorphous layer gives rise to secondary defects during the postimplant annealing due to the growth of the initially formed clusters and the movement of the amorphous/crystalline interface. Although the amorphous layer undergoes epitaxial regrowth during annealing, residual structures remain as observable defects within the lattice after recrystallization.

Figure 7 shows a TEM micrograph of the $p^+$ area close to the polysilicon gate of a p-channel device [11]. The source-drain areas have been formed by a single $BF_2$ implant. The formation of a band of defects can be noticed at a depth of 780Å, which is a factor of two deeper than the peak of the damage profile. The high density of defects in the junction areas has no negative impact on the device performance, because the junction is far away from the damage layer.

### IV. Device Results

#### 1. N-Channel MOSFETs

N-channel devices have been fabricated using a modified NMOS process [8]. For all levels, direct-write e-beam lithography has been used to achieve minimum active dimensions of 0.25$\mu$m [9]. Electrical results obtained from these devices have been extremely encouraging. Fig. 8 shows measured subthreshold currents as a function of gate voltage for two drain voltages (0.1, 1V) and several substrate voltages. The device dimensions are indicated in the figure. The device parameters obey the relationship in Fig. 1, which indicates that this scaling rule, albeit simple, is still valid for very small dimensions. The most encouraging result, however, is given by the current drive performance of these devices as shown in Fig. 9 [12]. The transconductance of this device is 300 mS/mm, the highest value ever obtained for any semiconductor structure at room temperature.

#### 2. P-Channel MOSFETs

As already mentioned above, the scaling of p-channel devices is more difficult. Nevertheless, p-channel devices with channel length as short as 0.5$\mu$m have been fabricated [13].The performance of these device is excellent as can be seen in Fig. 10 which compares the drive capabilities of n- and p-channel devices for the same bias conditions. For submicron dimensions, the p-channel device performance improves significantly due to the increased velocity of holes at high electric fields. This result allows important conclusions to be drawn for future submicrom CMOS technologies. The increased current drive of the p-channel device allows a considerable reduction of the gate area, which results in a significant decrease of the input capacitance.

### V. Conclusions

During the last few years, there has been large interest in the fabrication of very small MOSFET structures to explore the basic limitations of both fabrication techniques and device performance. This paper summarized recent experimental work on MOSFET scaling and submicron device technology. The results clearly show that the MOSFET, if properly scaled, shows excellent performance, suitable for future demands of VLSI.

#### Acknowledgment

The results reported in this paper are due to the combined efforts of many people in the Advanced LSI Development Laboratory at AT&T Bell Laboratories, Murray Hill. In particular, I would like to acknowledge E. N. Fuls and his group for their support in wafer processing , W. A. Johnson and his group for their support in lithography , S. M. Sze for originating the scaling work, and G. E. Smith and M. P. Lepselter for providing an environment which made all this work possible.

## REFERENCES


[1] J. R. Brews, W. Fichtner, E. H. Nicollian and S. M. Sze, *IEEE Electron Device Letters EDL-***1**, 2 (1980)

[2] K. K. Ng and G. W. Taylor, *IEEE Trans. ED-***30**, 871 (1983)

[3] R. J. Bayruns, P. I. Suciu, N. C. Wittwer, D. L. Fraser, E. N. Fuls, R. A. Kushner, F. R. Ashley and E. Gere, *IEEE J. SC-***17**, 367 (1982)

[4] M. P. Lepselter, D. S. Alles, H. J. Levinstein, G. E. Smith and H. A. Watson, *Proc. IEEE* **71**, 640 (1983)

[5] K. L. Tai, W. R. Sinclair, R. G. Vadimsky, J. M. Moran and M. J. Rand, 15th Symposium on Electron, Ion and Photon Beam Technology, Boston, MA (1979)

[6] J. R. Maldonado, M. E. Poulsen. T. E. Saunders, F. Vratny and A. Zacharias, *J. Vac. Sci. Technol.* **16**, 1942 (1979)

[7] D. R. Herriot, R. J. Collier, D. S. Alles and J. W. Stafford, *IEEE Trans. ED* **-22**, 385 (1975)

[8] W. Fichtner, in *VLSI Science and Technology 1984*, (K. E. Bean and G. A. Rozgonyi, eds.) The Electrochemical Society 1984

[9] W. Fichtner, R. K. Watts, D. B. Fraser, R. L. Johnston and S. M. Sze, *IEEE Electron Device Letters EDL-***3**, 412 (1982)

[10] W. Fichtner, E. Kinsbron and N. Lifshitz, Electrochemical Society Fall Meeting Extended Abstracts Vol 81-2 (1981)

[11] W. Fichtner, R. M. Levin, T. T. Sheng and R. B. Marcus, 161st Electrochemical Society Meeting, Montreal, Canada 1982

[12] W. Fichtner, E. N. Fuls, R. L. Johnston, R. K. Watts and W. W. Weick, 1983 IEDM Technical Digest, p. 384.

[13] W. Fichtner, R. M. Levin and G. W. Taylor, *IEEE Electron Device Letters EDL-***3**, 34 (1982)

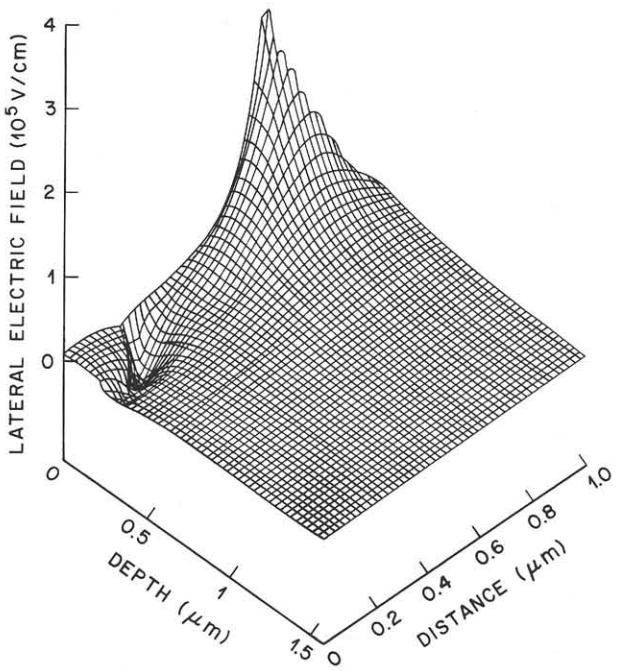




Fig. 2 Surface plot of the lateral electric field in the device as seen through the bulk. for $V_{gs}$=1V, $V_{ds}$=3V and $V_{bs}$=0.

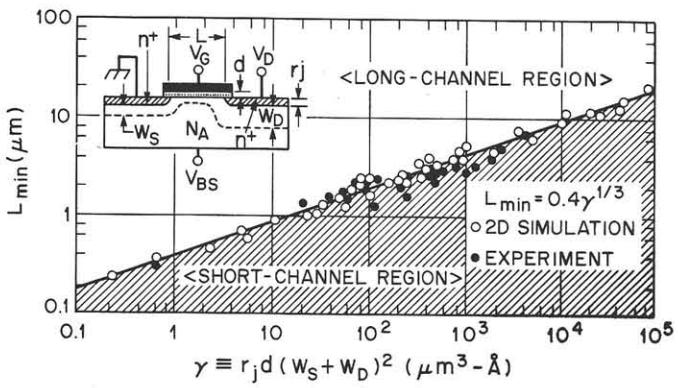



Fig. 1 Minimum channel length as a function of basic device parameters. For explanation see text and more detailed comments in [1].

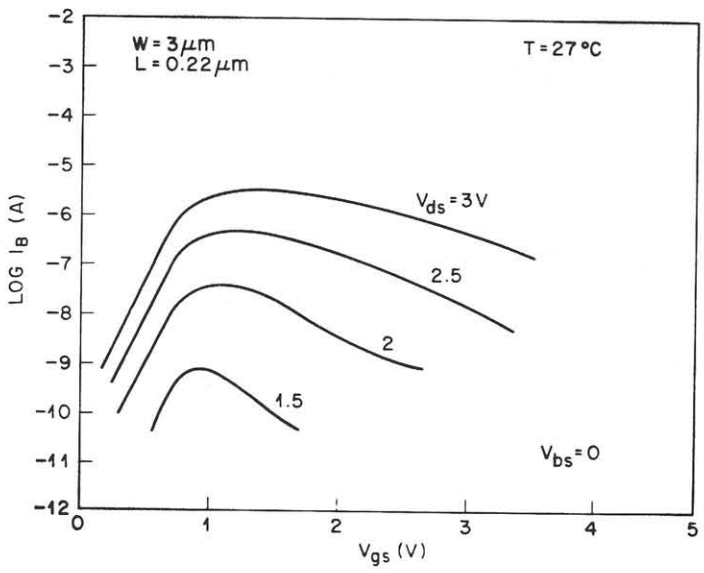



Fig. 3 Substrate current as a function of $V_{gs}$ for a n-channel device with $L$=0.22μm.

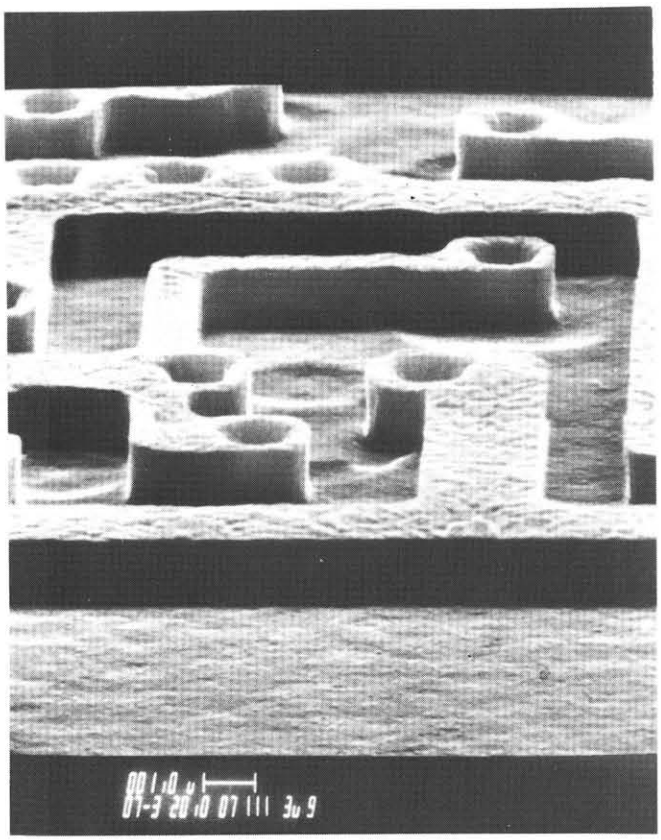


Fig. 4 SEM photograph of part of the metal level of a digital circuit fabricated using a 1$\mu$m NMOS technology.

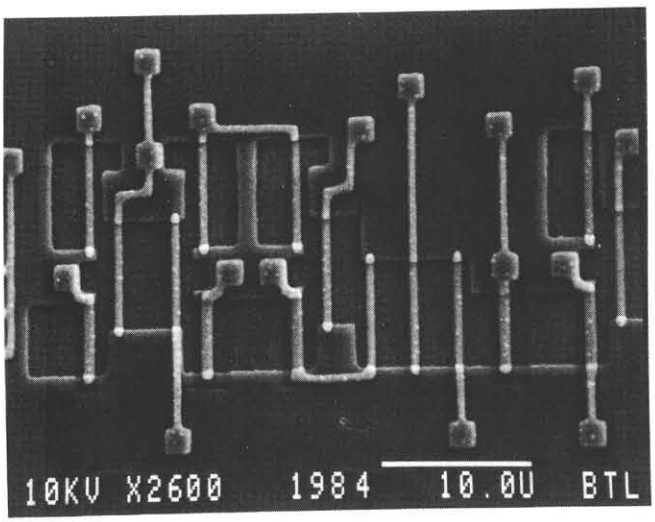
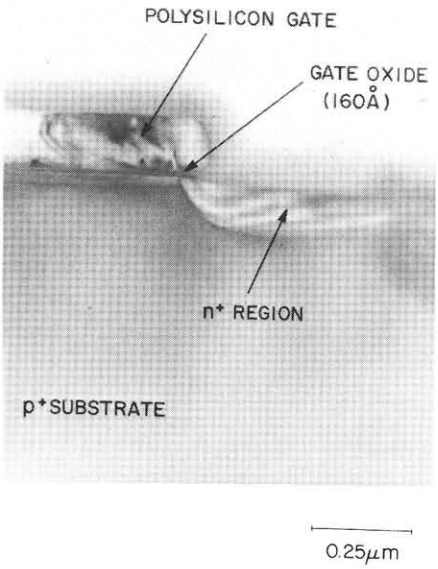



Fig. 5 SEM photograph of part of the polysilicon level of a counter circuit fabricated in 0.5$\mu$m NMOS technology.



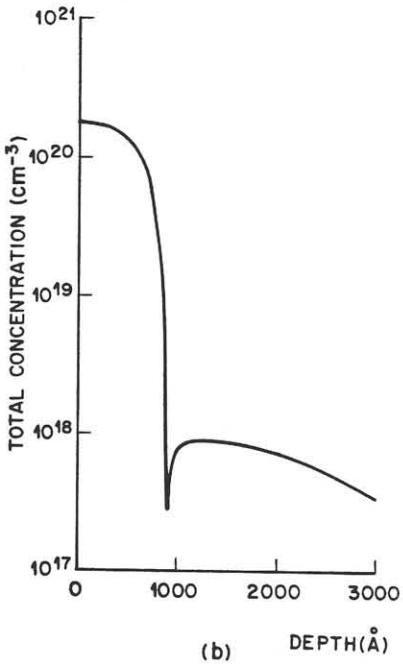




Fig. 6 (a)TEM micrograph of the cross section of the gate/junction area. (b) Depth profile of the arsenic in the junction area after drive-in.

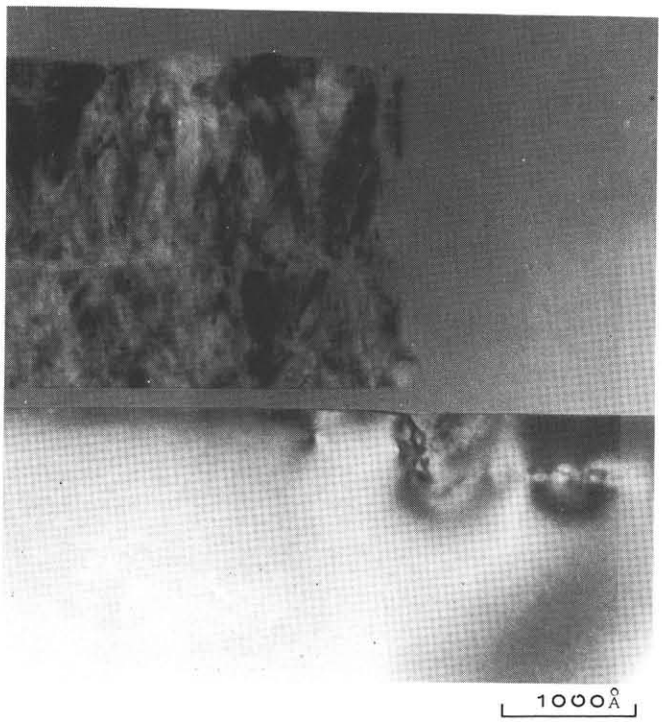



Fig. 7 TEM micrograph of a cross section of the gate/junction area of a submicron p-channel transistor.

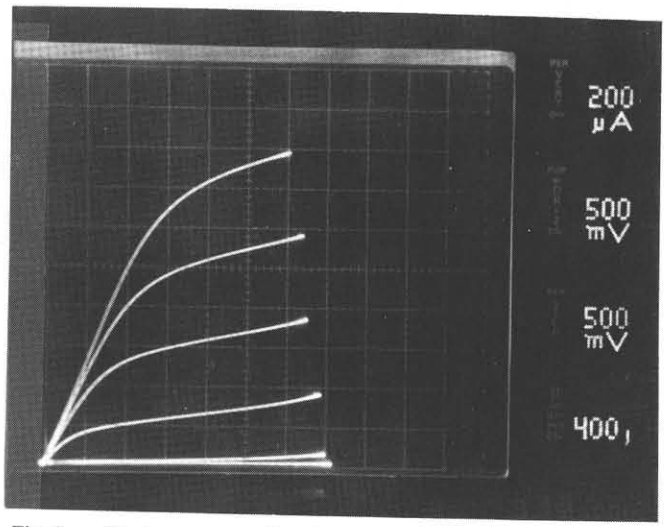



Fig. 9 Drain current as function of $V_{ds}$ for a n-channel device with $L$=0.22$\mu$m and $W$=3$\mu$m.

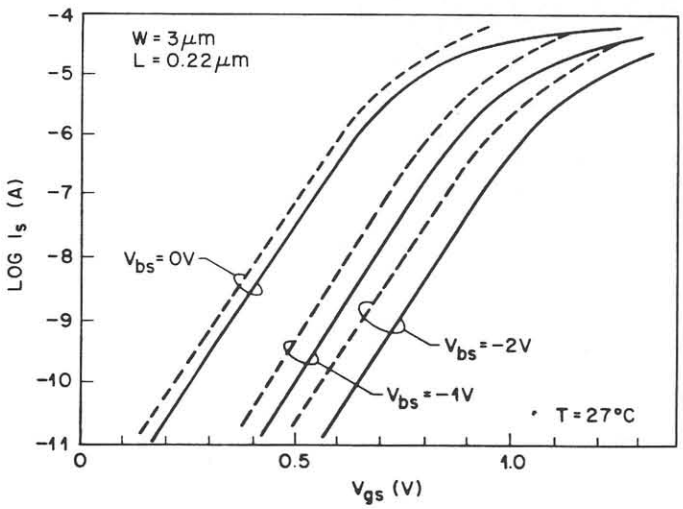



Fig. 8 Experimental subthreshold current as a function of $V_{gs}$ for a n-channel device with $L$=0.22$\mu m$.

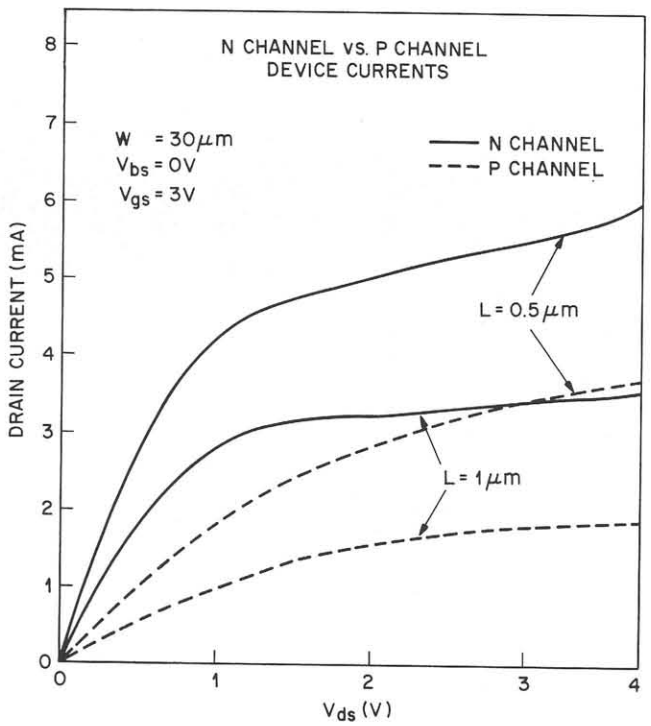



Fig. 10 Comparison of the drive currents as a function of absolute values for the bias voltages for two groups of n- and p-channel devices with channel lengths of 0.5$\mu$m and 1$\mu$m, respectively.