Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 83-86 **B-2-3**

Properties of Submicron Silicon MOSFET's from 300K to 4.2K*

Perry J. Robertson
David J. Dumin

Clemson University

Clemson, South Carolina 29631, USA

We have measured the characteristics of submicron silicon MOSFETs from 300K to 4.2K and plotted mobility versus temperature and carrier velocity versus longitudinal field as a function of temperature. We found effective mobilities in 500 μm devices as high as 25,000 cm^2/Vs at 4.2K. But mobilities in 0.2 μm devices were only 800 cm^2/Vs due to high field effects. We plotted mobility versus longitudinal field and found that ballistic transport is inhibited by the high fields in devices operating at 0.1 volts. Similar high field effects should limit the effects of ballistic transport in submicron GaAs FETs.

Background

In the past few years there has been a marked reduction in the minimum line definition achieved in microelectronic devices. This has reduced the minimum size of MOS transistors down below the 0.1 μm limit. Line widths of 25.0 nm are now possible due to the development of direct write-on-wafer e-beam technology coupled with better fine line photoresist polymers [1]. Modifications in the photoresist process have resulted in even smaller line widths [2].

As device sizes shrank, it was suggested by Shur and Eastman [3] that the effective channel length of these new submicron transistors might approach a size comparable to the mean free path the charge carriers in the channel. This would bring the transit time of these carriers down to the limit of the mean time between collisions. Thus, there would exist the possibility that electrons could be accelerated across the channel and be collected at the drain without scattering. Such an event has been termed "Ballistic Transport".

Much controversy has surrounded the exact nature of ballistic transport and the equations which would govern the affect [4]. In the classical sense, the motion of charge carriers through a semiconductor in the presence of a uniform electric field and in the absence of any scattering would be governed by [5].

$$Vs = \frac{q\,E\,t}{m^*} \tag{1}$$

where V_s is the effective velocity, q is the electron charge, E is the electric field, t is the transit time and m* is the effective electron mass.

Equation (1) has been used along with statistical methods to develop models which simulate the operation of a ballistic device. The majority of the models involve a Monte Carlo simulation of the ballistic process using various device structures, materials and doping densities [6-12]. But very little information has been published describing the results of experimental work performed in this area. Most of the experimental results have come from two-terminal GaAs diode structures [3] [13-15]. Even less has

* Work supported in part by the Office of Naval Research on contract No. N00014-81-U-0347.

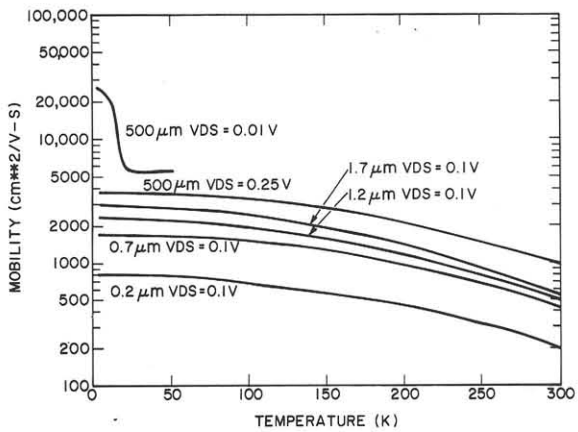

Figure 1. Mobility vs temperature for submicron and long channel transistors from 300K to 4.2K. Mobilities are progressively higher for lower longitudinal fields.

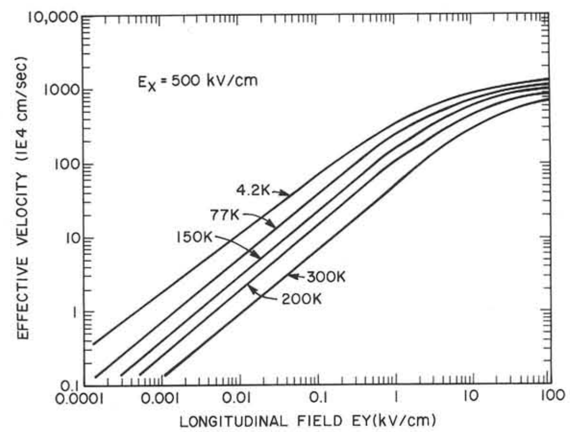

Figure 2. Effective electron velocity vs longitudinal electric field for temperatures from 300K to 4.2K. Relationship is linear below 1 kVicm. Saturation velocity is slightly higher at 4.2K.

been published relating to the possible occurrence of ballistic transport in silicon MOSFET devices either at room temperature or at cryogenic temperatures.

In this paper, we try to supplement the information available concerning submicron silicon MOSFETs and their relationship to ballistic transport. Secondly, we try to use our observations in silicon devices to predict the behavior of supposedly ballistic submicron GaAs FETs.

Transistor Descriptions

The transistors characterized by us were silicon, NMOS devices made available to us by AT&T Bell Laboratories (BTL) and the Naval Research Laboratory (NRL). The BTL transistors were enhancement mode devices with channel dopings of $1X10^{17}cm^{-3}$. The gate oxide was measured to be 28 nm. These four devices were configured on one chip with a common source and gate. Each device had its own individual drain. The effective channel lengths, L, were found to be 0.2, 0.7, 1.2 and 1.7 µm long and 30 µm wide [16]. They were manufactured using the modified NMOS process reported by W. Fichtner et al [17] [18].

The NRL 500x500 µm MOSFET was used as a long channel comparison device. This transistor was produced on a p-type, 15 Ω-cm silicon substrate and had a phosphorus doped, polysilicon gate grown over an 85 nm thick gate oxide. This gate was not self aligned. This transistor was characterized as having a very large low field channel mobility at 4.2K.

Effective Mobility

The drain current versus gate voltage curves for each device were measured for temperatures from 300K to 4.2K in the subthreshold, linear and saturation regimes. From these data, we were able to plot effective mobility versus transverse electric field curves for each device from 300K to 4.2K. Above about Ex = 500 kV/cm, μ_n fell off to a saturation value that was dependent upon the longitudinal electric field, Ey. With Vds = 0.1 volts, the saturation mobility varied from 100 cm^2/Vs with L = 0.2 µm to 400 cm^2/Vs with L = 1.7 µm. Using the value of mobility at a transverse field of 500 kV/cm for a variety of temperatures, we were able to plot the effective electron mobility of six different MOSFETs versus temperature as shown in Figure 1.

A comparison of the respective mobilities at 300K and 77K shows an increase factor of approximately four. This is in good agreement with published results for long channel transistors [19]. The mobility continued to increase with decreasing temperature down to 4.2K. This is not the same behavior as predicted for bulk silicon [20, p.30] [21] but is characteristic of surface transport. An uncharacteristicly large mobility was reported by Nelson Saks of NRL for one of the 500 µm transistors. With a longitudinal field of 0.2 V/cm, he measured an effective mobility of 25,000 cm^2/Vs at 4.2K. Achieving such a field (and thus a high mobility) in a practical 0.1 µm device would require an impractically small drain-to-source voltage.

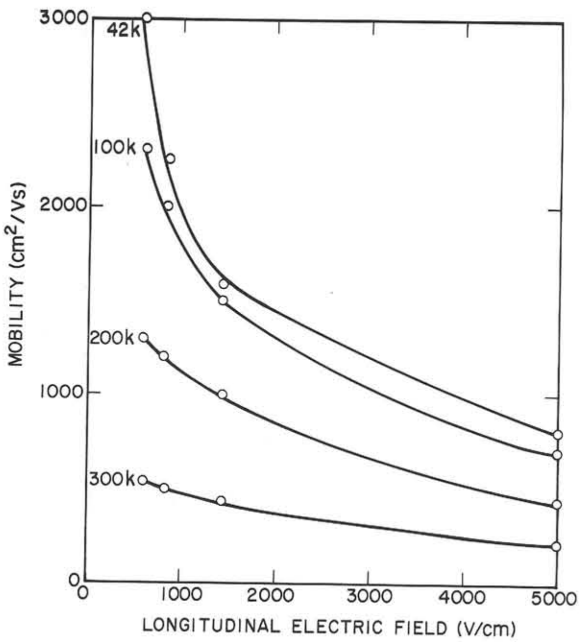

Figure 3. Effective electron mobility vs longitudinal electric field for temperatures from 300K to 4.2K. Reduction in movility at high fields is 73% at 4.2K versus 62% at 300K. The relationship between μ and Ey is almost hyperbolic at 4.2K.

Electron Drift Velocity

Using our transistor data we have plotted effective electron velocity versus longitudinal electric field for temperatures from 300K to 4.2K as shown in Figure 2. This data was taken with Ex=500 kV/cm.

The relationship between drift velocity and electric field in Figure 2 is linear below 1 kV/cm. The slope for thetemperatures 300K, 77K and 4.2K are 1.14, 1.19 and 1.26 respectively. The slope of the linear approximation to the lines in the low field region is the mobility as defined by $v_s = \mu_n E_y^S$, where v_s is the drift velocity, μ_n is the effective electron mobility and E_y is the longitudinal electric field (if we assume S = 1, which is a good approximation in our cases). This mobility is then 1000, 4,300 and 10,000 cm^2/Vs at 300K, 77K and 4.2K respectively. Our values for mobility are consistent with other published data at 300K. Finally, we did observe a slight increase in the saturation velocity at 4.2K as predicted by Sze by [20, p.46].

Mobility Reduction in High Fields

Using the data from Figure 1, we have plotted effective mobility versus longitudinal electric field for 300K, 200K, 100K and 4.2K as shown in Figure 3. We see that there is a much larger drop in mobility as one goes to higher fields at 4.2K (73%) than there is at 300K (62%). The high field effect is much more dominate at low temperatures. We also see an almost hyperbolic relationship between mobility and longitudinal electric field at 4.2K. This would predict the large jump in the effective mobility we saw in the 500 μm transistor operating at low temperatures and low electric fields.

It is easy to see how one could achieve a mobility of 10,000 cm^2/Vs or higher in silicon at low temperatures. But high fields such as the ones in submicron devices lower the effective mobilities dramatically.

Ballistic Transport

We see that devices operating at a higher longitudinal field have a lower effective mobility and thus a smaller mean free path. Even with Vds as small as 0.1 volts and gate lengths on the order of 0.2 μm the mean free path in silicon is much shorter than the gate length and these devices do not operate ballistically even at 4.2K. It is evident that in order to get a mean free path in a 0.2 μm device of the same order of length as found in the 500 μm device (and thus have the possibility of ballistic transport) one has lower Vds to a few microvolts. But noise margin considerations prevent operation of these devices at smaller Vds in practical MOS devices.

We feel that this limiting of the effective mobility will be found in 0.1 μm GaAs devices as they become available for testing. Even though noise margin constraints will allow for smaller drain-to-source voltages in GaAs devices, the operating point will still be above the high field point at which we see limiting of the effective mobility. We predict, then, that ballistic transport will not be an important phenomena in the operation of submicron GaAs FETs.

Conclusions

In conclusion, we have measured the I-V characteristics of submicron silicon MOSFETs from 300K to 4.2K in the subthreshold, linear and saturation regimes. We have obtained the mobility versus transverse electric field data for submicron devices in the linear and saturation. We used data from devices with gate lengths of 0.2, 0.7, 1.2, 1.7 and 500 μm to determine the effective electron drift velocity versus longitudinal electric field.

We found mobilities in 500 μm silicon devices that were as high as 25,000 cm^2/Vs at 4.2K. This was in the low field regime with Vds = 0.1 v were only about 800 cm^2/Vs at 4.2K. We saw that the shorter channel lengths lead to proportionally higher longitudinal electric fields which reduce the electron mobility in the channel. Therefore, the drain-to-source voltage would have to be reduced to a few microvolts to achieve mobilities high enough to observe ballistic transport in submicron devices.

We found that the effective electron velocity is linearly related to the longitudinal electric field for fields below 1000 V/cm. Above this point, the velocity begins to saturate just as in bulk material at a velocity of 10^7 cm/sec. The saturation velocity was slightly higher for lower temperatures. In the linear region, Ex=10,000 V/cm, we found that the mobility varied from 1000 and 4300 cm^2/Vs at 300K and 77K to 10,000 cm^2/Vs at 4.2K. Finally, we have shown that the high electric fields in submicron devices reduce the effective electron mobility in the channel by 62% at 300K and 73% at 4.2K. We expect that this high field effect will likewise limit the effective mobility of FETs made from high mobility materials such as GaAs.

We would like to thank Earnest Labate of AT&T Bell Laboratories, Nelson Saks of the Naval Research Laboratories, A. Ipri of RCA Laboratories and Pallab Chatterjee of Texas Instruments for the transistors used in this project. We would like to acknowledge Larry Cooper and the Office of Naval Research for their support.

References

[1] A. N. Borers, J. M. E. Harper and W. M. Molzen, Applied Physics Letters, Vol. 33 p. 392, 1978.
[2] A. N. Borers, W. M. Molzen, J. Cuomo, N. Wittels, Applied Physics Letters, Vol. 29, p. 596, 1976.
[3] M. S. Shur and L. F. Eastman, IEEE Electron Device Letters, Vol. EDL-3, No. 12, pp. 373-375.
[4] R. O. Grondin, P. Lugli, D. K. Ferry, IEEE Electron Device Letters, Vol. EDL-3, No. 12, pp. 373-375.
[5] S. L. Teitel and J. W. Wilkins, IEEE Trans. on Electron Devices, Vol. ED-30, No. 2, pp. 150-153.
[6] Y. Awano, et al, Electronics Letters, Feb. 4, 1982, Vol. 18, No. 3, pp. 133-135.
[7] K. Tomizawa, Electronics Letters, Aug. 18, 1983, Vol. 19, No. 17, pp. 697-698.
[8] Y. Awano, et al, Electronics Letters, Jan. 6, 1983, Vol. 19, No. 1, pp. 20-21.
[9] K. Tomizawa, et al, Electronics Letters, Dec. 9, 1982, Vol. 18, No. 25, pp. 1067-1069.
[10] K. Tomizawa, et al, IEEE Proceedings, Vol. 129, Pt. 1, No. 4, Aug. 1982, pp. 131-136.
[11] Ken Yamaguchi, IEEE Trans. on Electron Devices, Vol. ED-26, No. 7, pp. 1068-1074.
[12] Y. Awano, et al, IEDM, 1983.
[13] L. F. Eastman, Electronics Letters, June 19, 1980, Vol. 16, No. 13, pp. 524-525.
[14] R. Zuleeg, IEEE Electron Device Letters, Vol. EDL-1, No. 11, pp. 234-235.
[15] M. S. Shur and L. F. Eastman, Electronics Letters, Vol. 16, No. 13, pp. 522-523.
[16] John Chern, et al, IEEE Electron Device Letters, Vol. EDL-1, No. 9, pp. 170-173.
[17] W. Fichtner, R. K. Watts, D. B. Fraser and R. L. Johnston, IEEE Electron Device Letters, Vol. EDL-3, No. 12, pp. 412-414.
[18] W. Fichtner, et al, IEDM, 1982.
[19] S. K. Tewksbury, IEEE Trans. on Electron Devices, Vol. ED-28, No. 12, pp. 1519-1529.
[20] S. M. Sze, "Physics of Semiconductor Devices", (John Wiley & Sons, NY, 1981).
[21] C. Jacoboni, et al, Solid-State Electronics Vol. 20, pp. 77-89, 1977.