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Expectable Performances of Future NMOS and CMOS Technologies

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A general approach is proposed to determine performances that could be achieved with future submicron NMOS and CMOS technologies. It is based on the automatic optimization of the electrical and geometrical parameters of logical gates so that speed be as high as possible while taking into account some constraints to insure a good working of devices. This approach is applied to NMOS and CMOS technologies for effective channel lengths of 1, .5, .25 and .125 µm. The results are compared with some experimental performances.

1. INTRODUCTION

The success of MOS devices scaling [1] comes mainly from the increase of density which leads to an increase of circuit complexity and especially a reduction of costs. Further these benefits come with a very interesting improvement in circuit performances that we have studied in view of a future continuity of scaling trends.

However the scaling suffers from the existence of parasitic effects [2] which play an increasingly important role in limiting the gains. Generally in the literature the authors study MOS devices scaling limits which result from these parasitic effects [3, 4] and the corresponding performances [5] separately or successively.

In this paper a general approach is proposed based on the simultaneous study of limiting effects and performances. Its feature is to maximize the speed of a given technology under constraints to insure a good working at the device level (no punchthrough, threshold voltage, hot carrier effects...) and at circuit level (noise margins, logical levels, power consumption), taking into account the limiting parasitic effects (series resistances, saturation velocity of carriers, ...). The results are function of design rules, thus are dependent on the possibilities of the future fabrication equipment.

2. PROGRAMS OF AUTOMATIC SCALING

We have developped two programs, POPSI and OPEC, for the optimization of electrical and geometrical parameters of logical gates realized in NMOS and CMOS technologies respectively. They contain the following modules :

1 - description of the scenario
2 - constraints checking
3 - models of parasitic effects and active devices
4 - iterative optimization of parameters
5 - calculation of the cost function
6 - outputs

The description of the scenario includes design rules, the list of parameters to optimize and their allowed variation range, the values of other given parameters and data relative to constraints.

The calculation of the channel doping profile required to suppress punchthrough current, is performed in module 3. Its efficiency has been verified by the realization of optimized MOS transistors with channel lengths down to .22 um (figure 1).

These devices have been also used to validate an analytical model of S-D MOS current which accounts for the saturation velocity of carriers (figure 2), short channel effects and doping profile under the gate. The source and drain series resistances are calculated according to [6] and are taken into account iteratively.

The parameters optimization is performed by an exploratory search using a modified HOOKE and JEEVES method [7].

A great advantage of these programs is their modularity, so that it is easy to change models and constraints.

3. PERFORMANCES OF NMOS AND CMOS TECHNOLOGIES

In order to determine the performances that could be achieved with future submicron NMOS and CMOS technologies we have considered optimistic and pessimistic scenarios for each of the following channel lengths : 1, .5, .25 and .125 µm :

- optimistic scenarios are based on the scaling of given reference design rules (table 1) taking implicitly into account future improvements of processing.
- pessimistic scenarios are also based on a scaling, but limited by the present possibilities

of process (table 2). Furthermore a low doped drain structure is considered to improve MOSFET reliability. The consequence is an increase of source and drain series resistances.

The optimization of electrical and geometrical parameters is performed for given values of average static power for NMOS technology (figure 3) or of dynamic energy for CMOS technology (figure 4), in the case FI = FO = 1.

For each point of these curves we have optimized the following parameters :

- doping profiles under the channels of the different kinds of devices
- channel widths
- oxide thickness
- supply voltage

A larger difference between optimistic and pessimistic scenarios is observed when channel length decreases. This is due mainly to the fact that some parasitic capacitances are not fully scaled in the pessimistic scenario.

The existence of optimized values of parameters has been verified for the supply voltage, figure 5, where we try to minimize propagation delays for given values of dynamic energy and supply voltage.

Otherwise these results are valid for more complex circuits, because the values of optimized parameters are very near those obtained on loaded logical gates (FI = FO = 3).

4. EXPERIMENTAL RESULTS

To compare these expectable performances with some experimental ones, submicron N.MOS and C.MOS, 101 stages ring oscillators were realized using a step and repeat machine. Device parameters are given in table 3.

Typical results are propagation delay of 125 ps and average static power consumption of .45 mW for NMOS technology at 3V supply voltage. The C.MOS technology propagation delay is 160 ps for a dynamic energy of .56 pJ and 5 V supply voltage.

For smaller devices, there is also a good agreement between predicted performances and the best ones given in the literature : 30 ps at room temperature on a .25 µm channel length N.MOS technology [8].

5. SUMMARY

A general approach has been proposed to optimize the electrical and geometrical parameters of a given technology with logical gates speed as a criterion. This approach has been applied to submicron N.MOS and C.MOS technologies. We can conclude that, depending on the possibilities of the future fabrication equipment, very high performances are expectable. Further, due to its better scalability and lower power consumption compared with N.MOS, C.MOS will be the dominant technology.

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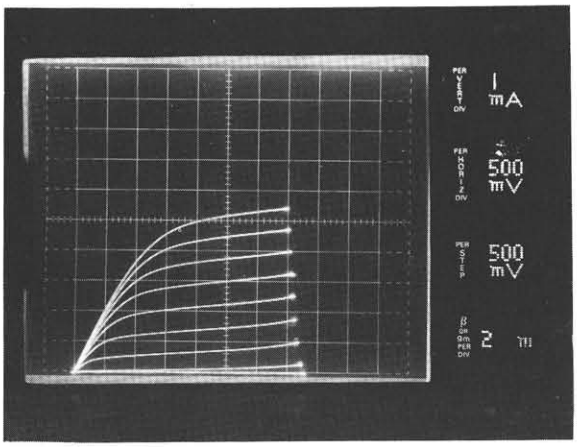

Fig 1 : OUTPUT CHARACTERISTICS
Channel length .22µm
Channel width 8.5µm
Oxide thickness 12nm
Threshold voltage .45V
Direct write e⁻ beam lithography

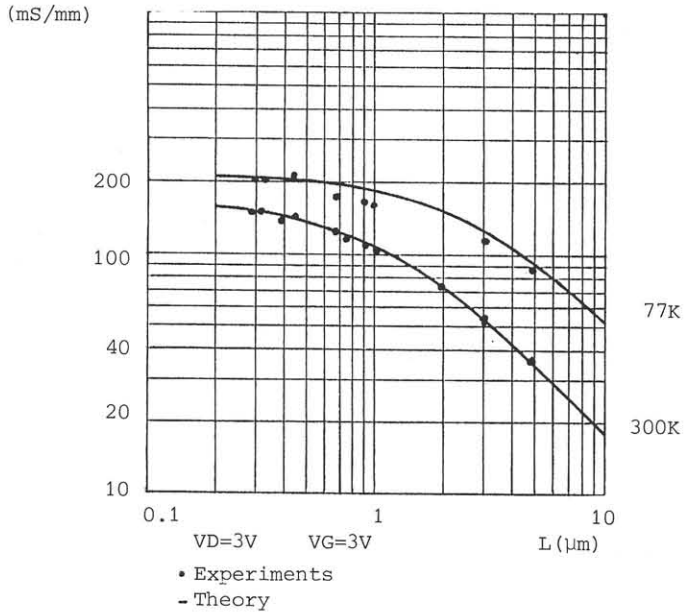

Fig 2 : TRANSCONDUCTANCE VS. CHANNEL LENGTH

Channel length	.8 µm
Poly-Si (Width/Spacing)	1µm/1µm
1st Al (Width/Spacing)	1.4µm/1µm
1st Contact hole	1µm x 1µm
Misalignment	.25µm

Table 1 : DESIGN RULES FOR A 1µm TECHNOLOGY

1st Contact hole	>	.5µm x .5µm
Misalignment	>	.2µm
Junction depth	>	.2µm
Gate-Drain overlap	>	.1µm
Contact hole to gate distance	>	.4µm

Table 2 : LIMITATIONS OF PROCESS POSSIBILITIES FOR PESSIMISTIC SCENARIOS

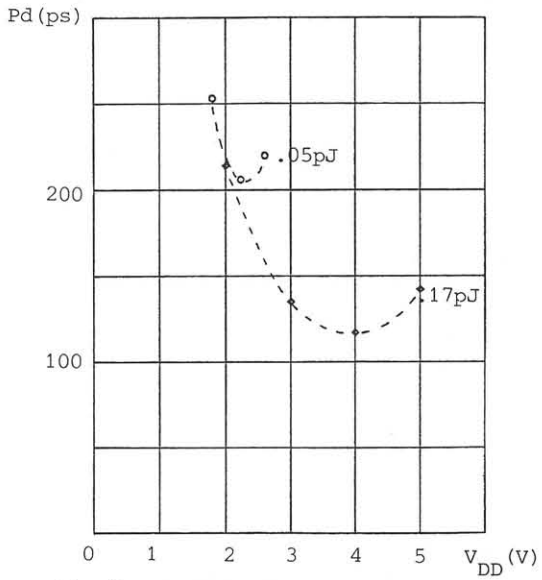

Fig 5 : EXPECTABLE PROPAGATION DELAY AS A FUNCTION OF SUPPLY VOLTAGE TAKING THE DYNAMIC ENERGY AS A PARAMETER
- .5µm channel length
- pessimistic scenario

	N.MOS		C.MOS	
Parameter	Enhancement	Depletion	N Channel	P Channel
Gate oxide thickness (Å)	250	250	250	250
Channel length (µm)	.8	.8	.6	.6
Channel width (µm)	7.5	4	2.5	2.5
Junction depth (µm)	.21	.21	.25	.25
Threshold voltage (V)	.63	-1.5	.6	-.7

TABLE 3 : DEVICE PARAMETERS

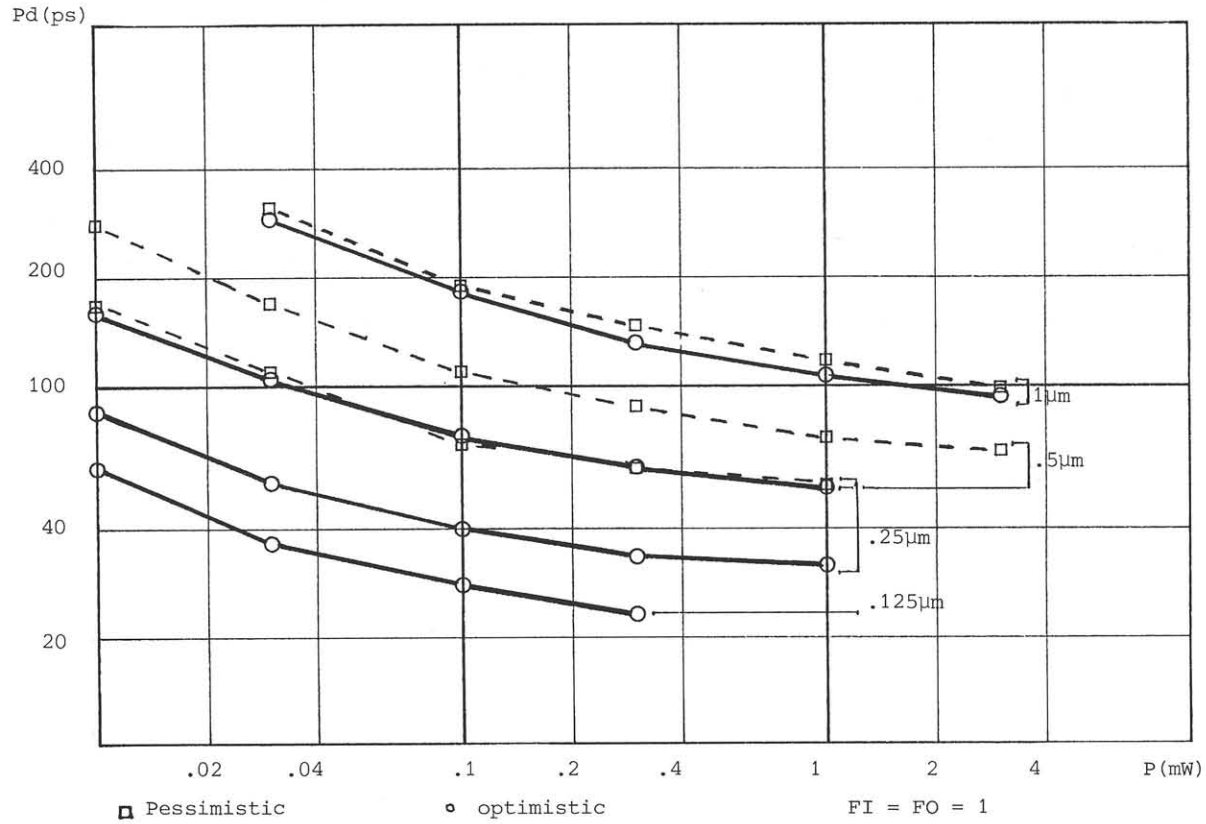

Fig 3 : EXPECTABLE PROPAGATION DELAY OF NMOS TECHNOLOGY AS A FUNCTION OF AVERAGE STATIC POWER CONSUMPTION TAKING THE CHANNEL LENGTH AS A PARAMETER

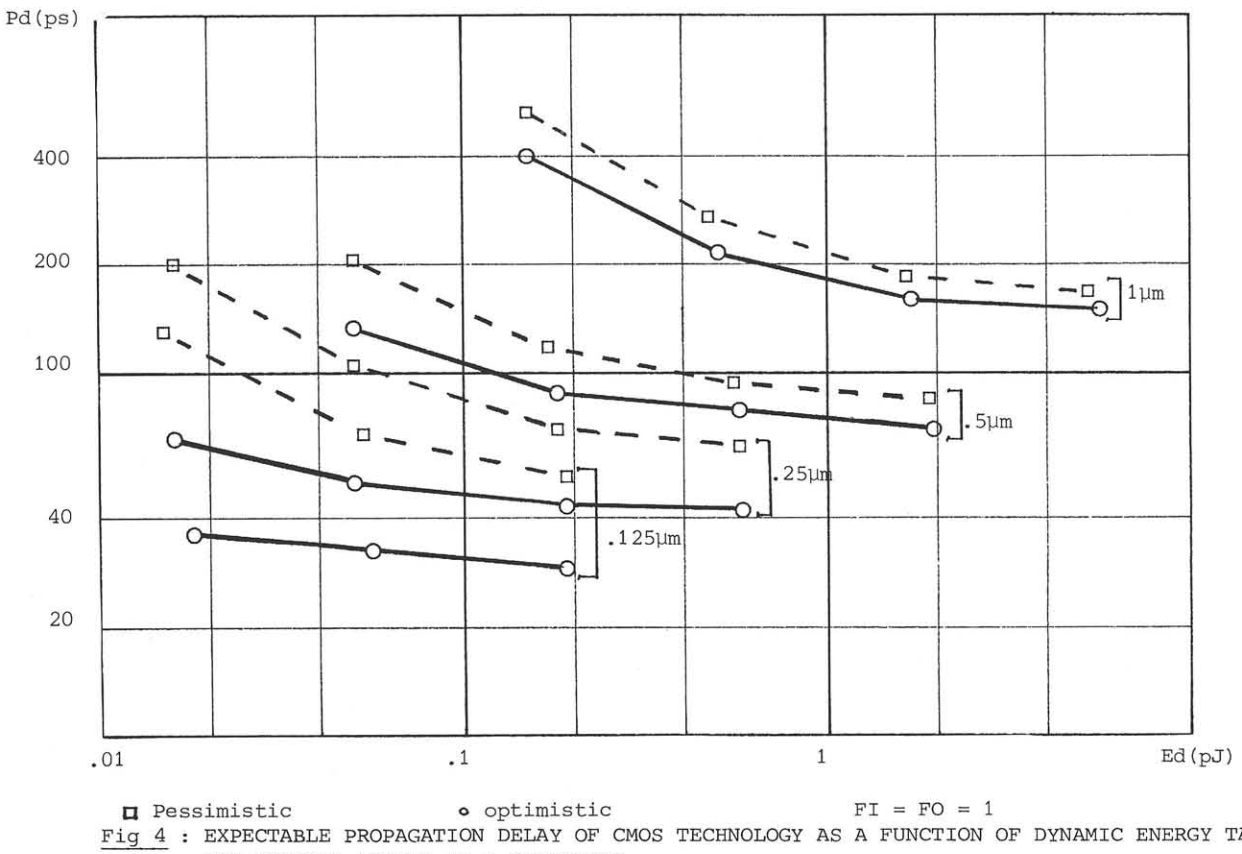

Fig 4 : EXPECTABLE PROPAGATION DELAY OF CMOS TECHNOLOGY AS A FUNCTION OF DYNAMIC ENERGY TAKING THE CHANNEL LENGTH AS A PARAMETER