Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 111-114

Enhanced Impurity Redistribution for Silicided Source/Drain

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The redistribution of impurities during Mo and Ti silicide formation has been studied. It has been revealed by SIMS measurements and I-V characteristics of pn junction that impurity profiles are enhanced by crystal defects at the metal/Si interface. Thus impurity profiles after silicidation are strongly affected by silicidation temperature and ion implantation conditions. Utilizing enhanced impurity redistribution phenomena, excellent silicided pn junction and high performance submicron CMOSFETs have been fabricated.

§1 INTRODUCTION

To stably form shallow n^+ and p^+ regions with low sheet resistivity is indispensable to submicron CMOS device fabrication[1]. However, using ion implantation technique, it is very difficult to realize shallow junction, consisting of high concentration layers, because of restriction of diffusivity and solid solibility. Even if shallow junction could be obtained, the severe problems would remain to prevent Al penetration into silicon. Silicided source/drain structure, which is one of the promised technologies, has been proposed to meet these requirements. For silicided source/drain, it is needed to form low leakage pn junctions possesing both low sheet resistivity and silicide/Si contact resistivity[2),3)]. Thus it is necessary to realize controlled impurity profile and higher impurity concentration layers at the silicide/Si interface ;the former is for low leakage pn junction and the latter for low contact resistivity.

In this study, it has been clarified that both annealing and ion implantation conditions strongly affect silicided impurity profiles of pn junction. By physical and electrical analyses impurity diffusion behaviors are investigated. As a result, it has been confirmed that the defects at the metal/Si interface enhance impurity redistribution during silicide formation. Moreover utilizing enhanced impurity redistribution, higher performance submicron n and p channel MOSFETs have been fabricated succesfully.

§ 2 EXPERIMENTAL PROCEDURES

The P type and N type silicon wafers were used as substrates to fabricate pn junctions and MOS devices. Molybdenum (Mo) and Titanum (Ti) films were deposited using sputtering on Si wafers after removal of native oxide by dilute HF. After the metal deposition (50nm), As^+ and Si^++B^+ impurities were implanted through the metal films under the condition that the peak of implanted profile reaches to the metal/Si interface as listed in Table 1. Heat treatment was carried out in N_2+H_2 ambients to form silicide.

To analize impurity profiles, SIMS (Secondary Ion Micro Spectroscopy) measurements were performed, and both I-V characteristics of pn diode for leakage currents and that of silicide/Si contact for ohmicity were measured.

§3 RESULTS and DISCUSSION

3.1 IMPURITY PROFILES OF ENHANCED REDISTRIBUTION

Figure 1 and Fig. 2 show in-depth impurity profiles in Mo silicide/Si. The samples were heated at 600°C or 800°C after ion implantation. It is observed that the junction depth after 600°C annealing is deeper than that after 800°C annealing in Mo and Ti silicide. Furthermore it should be noted that arsenic redistribution can be observed

after 600°C annealing during Ti silicide formation, although C.Y.Ting et.al. have reported the lack in impurity redistribution[4].

Those results can not be explained by thermal diffusion mechanism, but they can be well explicated, taking account of defects at the metal/Si interface. Since during 600°C annealing the regrowth rate of amorphaized Si layer induced by ion implantation is nearly equal to the Mo and Ti silicide formation rate [5)-8)], the density of crystal defects at the metal/Si interface after 600°C annealing is much higher than that after 800°C annealing. Therefore it is very likely that the defects at the Mo/Si interface enhance impurity redistribution during silicidation[9]. Accordingly impurities redistribution after 600°C annealing is more remarkable than after 800°C annealing. This model has been also confirmed, considering that enhanced impurity redistribution can be caused by induced crystal defects at the metal/Si interface even in Ti silicide.

Thus, impurity redistribution during silicide formation is enhanced by the defects at the metal/Si interface. Therefore silicided pn junction profiles are strongly dependent upon silicide formation conditions such as ion implantation through the metal film and annealing temperature during silicidation.

3.2 ELECTRICAL CHARACTERISTICS

It is widely accepted that both impurity and damage profiles have strong influence on electrical characteristics of pn junction. Figure 3 shows process sequence for silicided pn diode fabrication. Figure 4 and Fig. 5 show measured results for reverse current of Mo and Ti silicided pn diode, which indicate As^+ and Si^+ ion implanted dose dependence.

Since the reverse current level depends upon the number of generation-recombination centers in the depletion layer, the leakage current reflects how pn junction exceeds the damaged layer. Hence the results show that the junction depth becomes deeper as the implanted dose increases; namely the defect density increases at the metal/Si interface. This means that the impurity diffusivity is more enhanced by crystal defects at the metal/Si interface, so that the generation-recombination center will not be mostly involved in the depletion layer. Particularly when implanted dose is 5×10^{15} cm^{-2}, the reverse current level is held as low as that of conventional pn junction.

Contact characteristics of silicide to N^+ and P^+ layers have also been investigated. Good ohmicity has been obtained in both cases of Mo silicide and Ti silicide as shown in Fig. 6. Moreover, high impurity concentration layers should be formed when enhanced impurity redistribution occurs during silicide formation, because ohmicity has been preserved up to 900° heat treatment even for Ti silicide.

Thus, it has been verified that the impurity profiles can be controlled and the preferable silicided pn junction profiles for CMOS devices can be realized, utilizing enhanced impurity redistribution during silicide formation. Consequently, excellent silicided pn junctions and ohmic contacts to silicide/diffusion layers have been obtained.

3.3 SUBMICRON CMOS DEVICE FABRICATION

CMOS devices with silicided source/drain and gate electrode have been fabricated by self alignment technique. Process parameters for n and p channel MOSFETs are as follows: typical oxide thickness is 20nm; Mo silicide thickness is 0.1um; sheet resistivity of source/drain is 10ohm/square; n^+ and p^+ junction depths are 0.15um and 0.22um, respectively. Figure 7 shows the drain current-voltage characteristics of n and p channel MOSFETs. It has been accomplished that the transconductance is increased owing to reduction of source/drain resistivity, and the subthreshold current is held as low as that of the conventional process.

§4 CONCLUSION

Enhanced impurity redistribution during silicidation has been studied. It has been verified that the impurity redistribution is enhanced by crystal defects at the metal/Si interface, and, hence, impurity profiles after silicidation are strongly affected by temperature for silicide formation and ion implantation conditions.

Moreover, by utilizing enhanced impurity redistribution, preferable impurity profiles can be obtained, so that excellent silicided pn diode and ohmic silicide/diffusion layer contact have been accomplishied.

This technology has been succesfully applied to submicron CMOSFETs and appears to be quite promising for submicron CMOS devices.

ACKNOWLEDGMENT

The authors wish to express their appreciation to Dr. S. Kohyama for his valuable suggestions and discussions.

REFERENCES

(1) H. Shichijo: Solid State Electron.**26**(1983)269.

(2) T. Shibata, K. Hieda, M. Sato, M. Konaka, R.L.M. Dang and H. Iizuka : IEDM Tech. Dig. (1981) p.647.

(3) H. Okabayashi, E. Nagasawa and M. Morimoto:IEDM Tech. Dig. (1982) p.556.

(4) C.Y.Ting, M.Wittmer and K.N.Tu : Electrochem. Soc. Fall Meeting, Extended Abst.(1982) p.242.

(5) L.S.Hung, J.Gyulai, J.W.Mayer, S.S.Lau and M-A. Nicolet: J. Appl. Phys. **54** (1983) 5076.

(6) Y.Liu, C.Lin and J.Maa : Jpn. J. Appl. Phys. **18** (1978) 991.

(7) S.Yanagisawa and T. Fukuyama:J. Electrochem. Soc. **127** (1980) 1150.

(8) S.S.Lau : THIN FILMS Ed. by J. Poate, K.N. Tu and J.W.Mayer (John Wiley& Sons Inc.,New York, 1978)p.433.

(9) G.J.van Gurp, J.W.Slotboom, F.J.B.Smolders, W.T.Stacy and Y.Tamminga : J.Electrochem. Soc. **127** (1980) 1813.

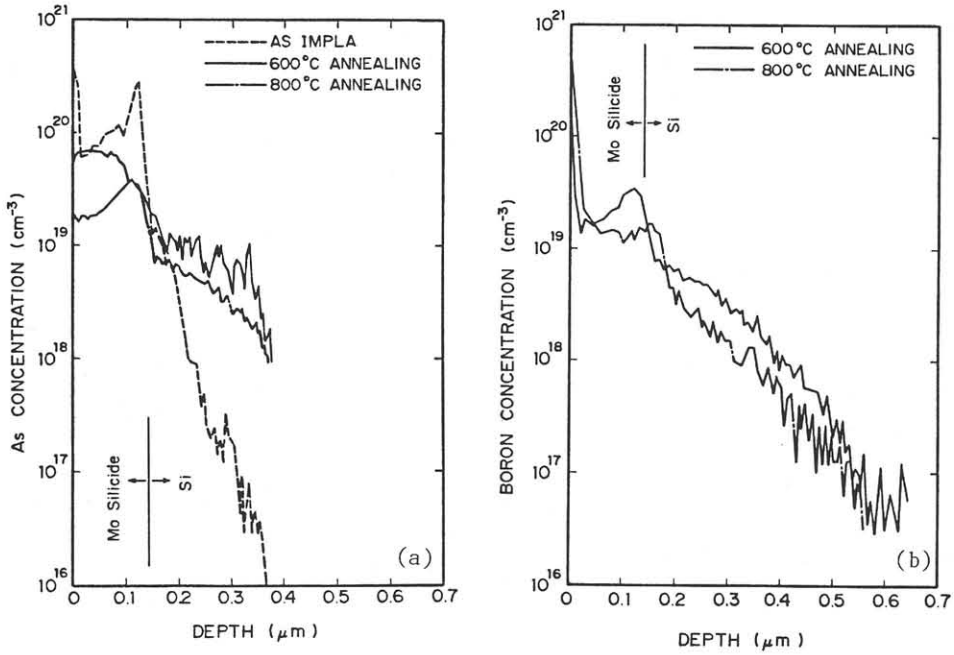

Fig.1 SIMS profiles of redistributed (a) arsenic and (b) boron in Mo silicide.

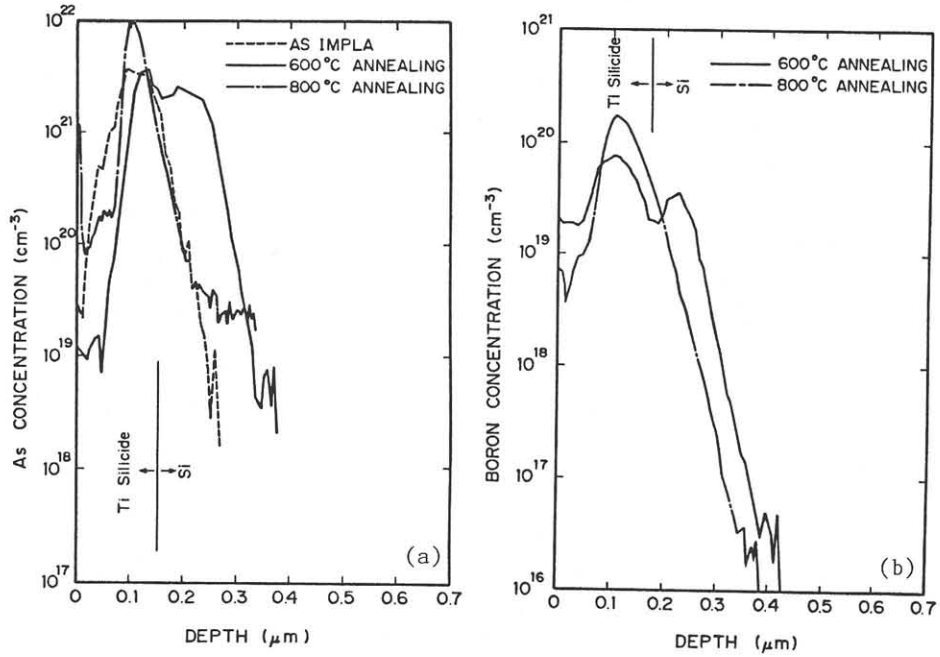

Fig.2 SIMS profiles of redistributed (a) arsenic and (b) boron in Ti silicide.

Table 1 Ion implanted conditions.

METAL	N type	P type
Mo	As^+ 160keV $2\sim5\times10^{15}cm^{-2}$	B^+ 35keV $3\times10^{15}cm^{-2}$ Si^+ 100keV $1\sim5\times10^{15}cm^{-2}$
Ti	As^+ 120keV $2\sim5\times10^{15}cm^{-2}$	B^+ 15keV $3\times10^{15}cm^{-2}$ Si^+ 50keV $1\sim5\times10^{15}cm^{-2}$

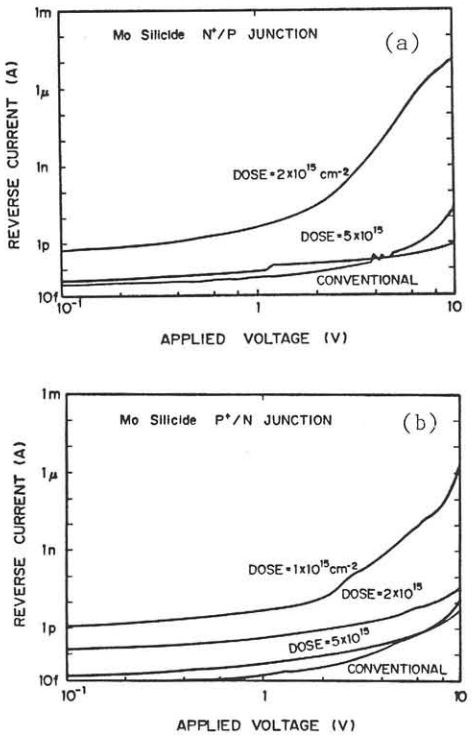

Fig. 4 Reverse current of Mo silicided pn junctionas a parameter of (a) arsenic and (b) silicon ion implanted dose.

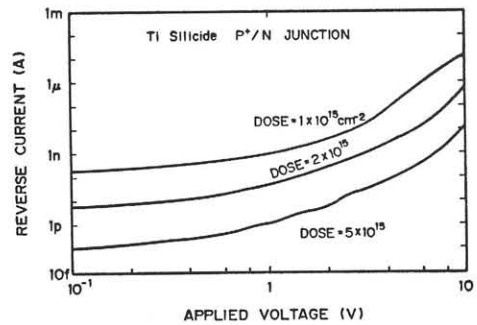

Fig. 5 Reverse current of Ti silicided pn junction as a parameter of silicon ion implanted dose.

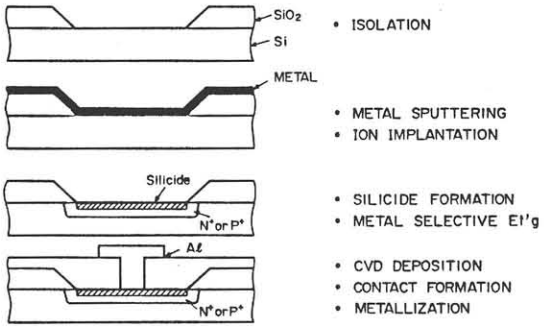

Fig.3 Process procedure of silicided pn junction.

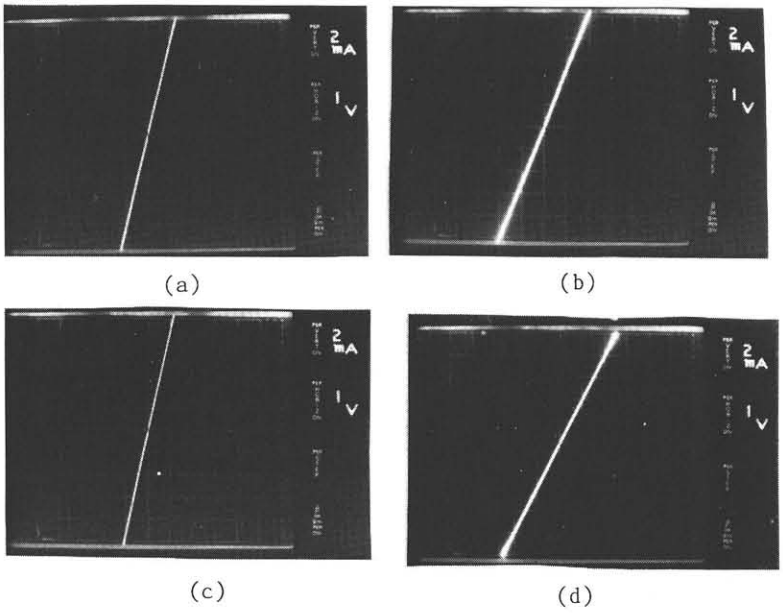

Fig. 6 I-V characteristics of silicide/Si contact.
(a) Mo silicide/n^+
(b) Mo silicide/p^+
(c) Ti silicide/n^+
(d) Ti silicide/p^+

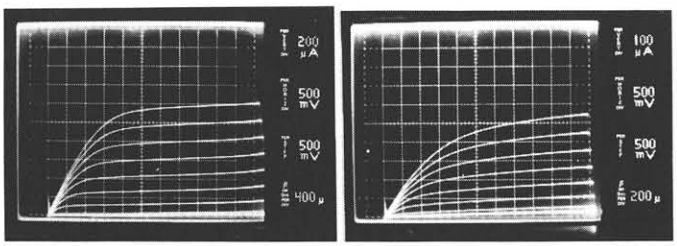

Fig. 7 Drain current v.s. drain voltage characteristics. Effective channeal length is 0.5um and channel width is 5um.
(a) n channel MOSFET
(b) p channel MOSFET