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A New Vertical Sidewall Channel Power MOSFET with Rectangular Grooves

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A new structure power MOSFET, in which the vertical sidewall channels are provided along the rectangular groove, is demonstrated. The new structure is featured by the high packing density and thereby the low on-resistance. A device with a 3.5 mm chip size exhibited an on-resistance of 30 mΩ and a breakdown voltage of 50 V.

§1. Introduction

Much attention in power MOSFET's have been paid to the vertical FET structures [1][2] represented by DMOS and VMOSFET's These power MOSFET's, however, suffers from the large on-resistance due to the low packing density.

In this paper, we demonstrate a new vertical power MOSFET which substantially possesses the higher packing density and thereby the lower on-resistance over those FET's.

The device with an on-resistance of 30 mΩ and a breakdown voltage of 50 V in a 3.5 mm x 3.5 mm chip has been successfully fabricated.

§2. Design consideration

A. Structure

A schematic cross section of the new vertical power MOSFET structure is shown in Fig. 1. The feature of the structure is that the gate is provided vertically along the sidewalls of the rectangular groove that penetrates into the n^- drain buffer region through n^+ source and p body regions.

The carrier flows from n^+ source to n^- drain bufler regions through the sidewall channel and the accumulation layer formed under the gate-drain overlap. The RIBE (reactive ion beam etching) technique is powerful to form rectangular grooves with excellent anisotropy [3].

B. 2-D numerical simulation

In order to investigate the potential profile and the carrier distribution in the rectangular groove structure, two dimensional computer simulation was done by solving the Poisson's equation. The simulation model used is shown in Fig. 2. The model uses the 60 x 70 points itrating the Stone's algorithm. The carrier distribution is calculated under the assumption that the quasi fermi levels are equal to the terminal voltages [4].

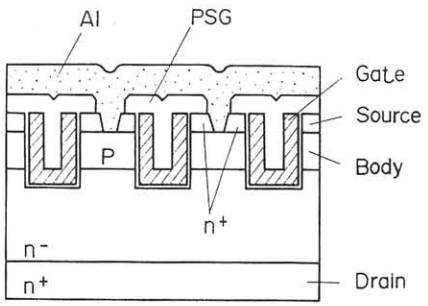


Fig.1. Schematic cross-section of new MOSFET.

The calculated results for potential and carrier distributions are shown in Fig. 3 and 4, respectively. The potential profile (Fig. 3) indicates that

1. There is no punchthrough near the groove.
2. The high electric field appears in the oxide of the gate-drain overlap.
3. Electric field convergence is observed near the corner of the rectangular groove.

The carrier distribution (Fig. 4) shows that the accumulation layer with a concentration over 1 x 10^{20} is formed under the gate-drain overlap. This means that the carriers from the channel is stored in this overlap region and spreads into the drain buffer region. Namely, the

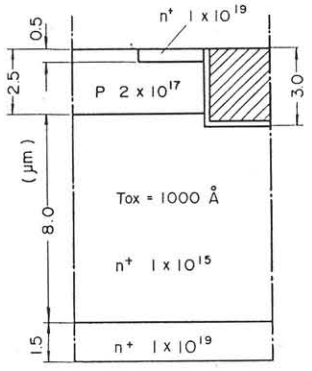


Fig.2. Simulation model.

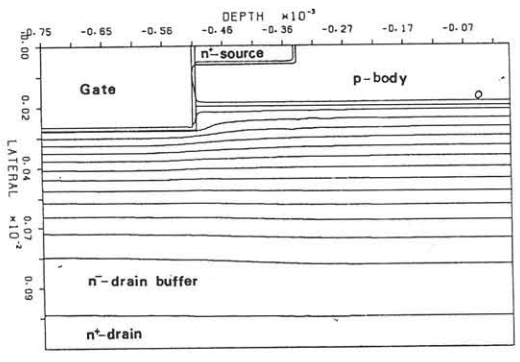


Fig.3. Calculated potential profile with applied drain voltage of 50 V.

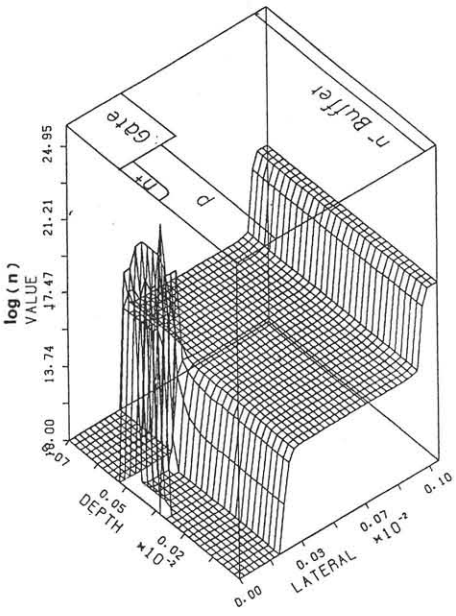


Fig.4. calculated carrier profile with gate voltage of 20 V.

new structure is well suited to reduce the resistance of the drain-buffer region because the overlap area is wider than those of any other conventioanl power MOSFET.

C. On-resistance

On-resistance R_{on} is given by the sum of the channel resistance R_{ch} and the resistance of the epitaxially grown drain-buffer region R_{epi}. The model used for calculating R_{on} is shown in Fig. 3. The formula for R_{ch} per unit area is given as a function of the groove pitch b because the total gate width is inversely proportional to the pitch. R_{epi} is calculated by integrating the hatched area in Fig. 5. The resultant formulae are written as,

$$R_{ch} = \frac{L_g \cdot b}{2 \mu_n C_{ox} (V_G - V_T)} \qquad (1\text{-a})$$

$$R_{epi} = \rho \left(\frac{b}{2} \log \frac{b}{a} + t - \frac{b-a}{2} \right) \qquad (1\text{-b})$$

where L_g : gate length

μ_n : surface electron mobility

C_{ox} : gate capacitance per unit area

V_G : applied gate voltage

V_T : threshold voltage

ρ : resistivity of the epi layer

t : thickness of the epi layer

R_{epi} of equ. (1-b) is calculated on the assumption that the epitaxial layer has the resistivity and the thickness to meet the theoretical breakdown voltage.

The on-resistance is numerically calculated as a function of breakdown voltage using the values shown in Table I. Fig. 6 shows that the on-resistance is dominated by R_{ch} in the low V_{DS} region and by R_{epi} in the high V_{DS} region. This concludes that increase of the packing density greatly contributes to the reduction of the on-resistance especially in the low breakdown voltage range.

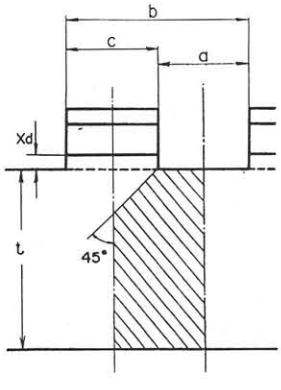


Fig.5. R_{on} calculation model.

Table I Prameters.

Rch	Lg	2 μm
	Cox	3.46×10^{-4} PF/μm²
	μn	500 cm²/v·s
	VG -VT	20 V
Repi	P	1 Ω·cm
	t	10 μm
	a	5 μm

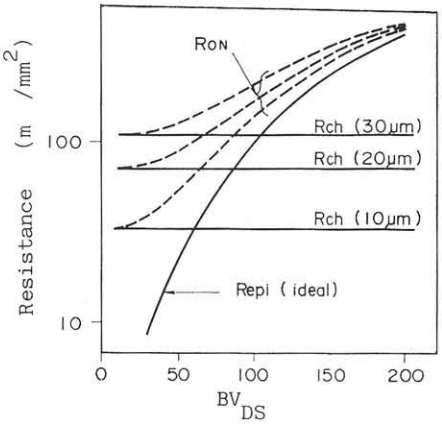


Fig.6. R_{on} v.s. breakdown voltage BV_{DS}.

§3. Device fabrication

The processing steps for the new structure power MOSFET are shown in Fig. 7. The starting material used was an n^-/n^+ silicon epitaxial wafer. The resistivity and the thickness of the epi layer were 1 Ω·cm and 10 μm, respectively. 7×10^{13} dose of B^+ ions were implanted to form the p body region and annealed to depth of 2.5 μm. 2×10^{15} dose of As^+ ions were implanted to form the n^+ source region. A Si_3N_4 and SiO_2 films with the thickness of 1000 Å and 2 μm, respectively, were deposited by the LPCVD technique (Step 1). It is to be noted that the thick SiO_2 layer was used as a etching mask for grooving. Rectangular grooving was performed by use of the RIBE technique at a pressure of 8×10^{-5} torr and a acceleration voltage of 1.5 kV using a mixed gas of $CCl_2F_2 + O_2$. Slight wet chemical etcing was applied to remove the damaged and contaminated surface of the groove (Step 2). The overhang appeared in the above etching process is completely removed by etching the SiO_2 layer before removing the Si_3N_4 film. In order to prevent the punchthrough of the p-body region, the impurity concentration of the p-body region was designed to be as high as 2×10^{17}. The threshold voltage was controlled by use of the boron segregation oxidation prior to the gate oxdation. After the gate oxidation with 1000 Å followed by the poly-silicon gate delineation, the groove was refilled with the glass flow of PSG (phosphosilicate glass) at a temperature of 1000 °C (Step 3). The oxide film and the underlying n^+ source region were successively etched off in order to make contacts for source and body regions simultaneously [6]. A sputtered Al-Si-Cu ternary alloys was used for the source and gate metalization (Step 4).

A SEM photomicrograph of the cross section of the fabricated device is shown in Fig. 8. A photograph of the fabricated power MOSFET mounted on To-3 package is shown in Fig. 9. The chip size was 3.5 mm x 3.5 mm.

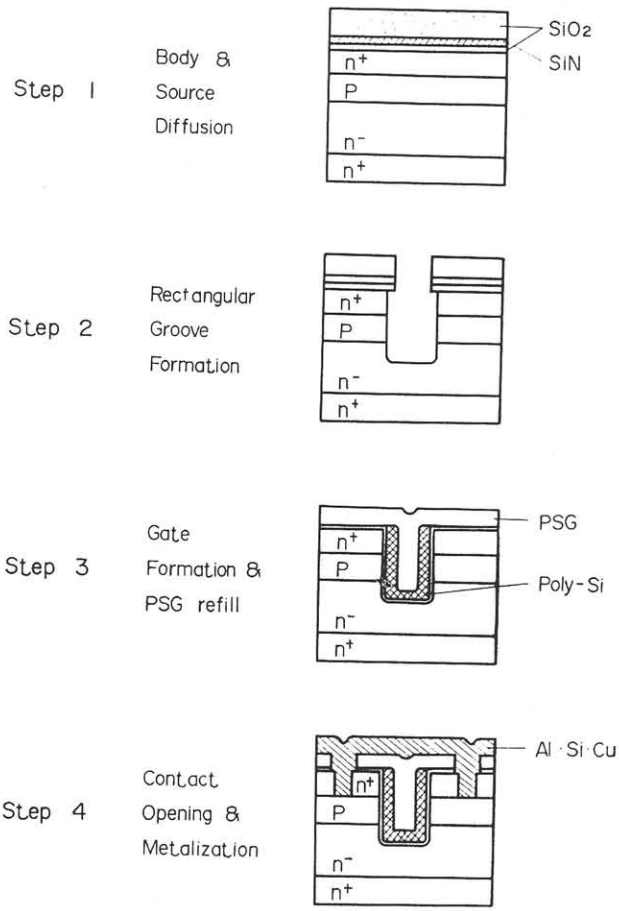


Fig.7. Process steps.

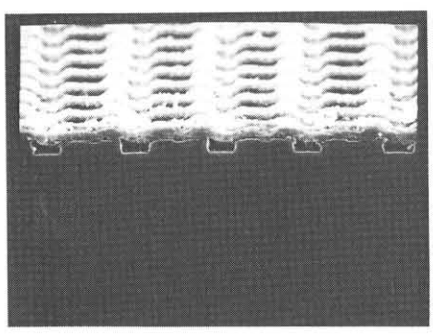


Fig.8. SEM photomicrograph of fabricated device.

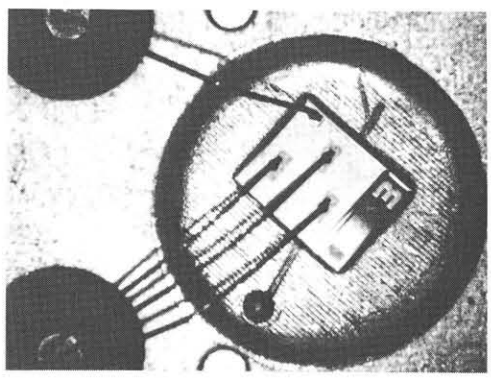


Fig.9. Photograph of fabricated chip mounted on To-3 package.

§4. Electrical characteristics and discussions

Typical I-V characteristics of the fabricated device are shown in Fig. 10, where an on-resistance of 30 mΩ is observed.

The measured input capacitance (Ciss), output capacitance (Coss), and reverse feedback capacitance (Crss) are 1980 pF, 2750 pF, and 1420 pF, respectively. This small input capacitance is due to the shorter channel length, thicker PSG film, and the small overlap area. It is also noted the output capacitance, which is proportional to the chip area, is quite small due to the high packing density.

Switching characteristics together with the measuring circuits are shown in Fig. 11, indicating that the rise and fall times are both less than 200 nS. This short swithcing time is attributed to smaller parasitic capacitances.

A comparison of the packing density and the on-resistance for VMOS and DMOS structures is made in TABLE II. The packing density of the new structure is limited neither by the width of the groove window nor by the diffusion length of the body region so that the largest gate width and lowest channel resistance can be obtained. The ideal R_{on} ratio is calculated assuming a 3 μm design rule with a negligible drain buffer resistance.

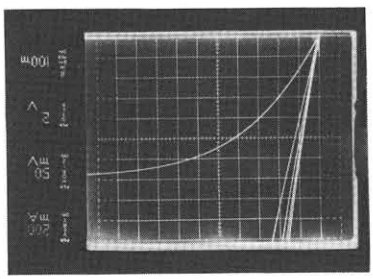
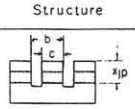
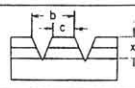
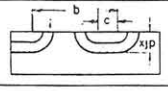
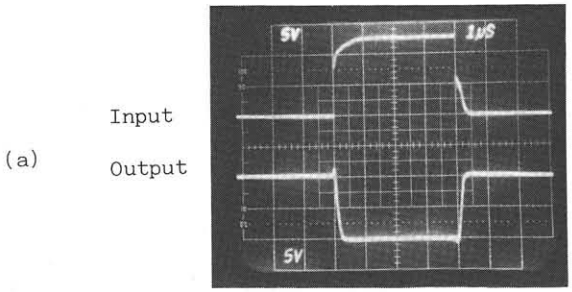


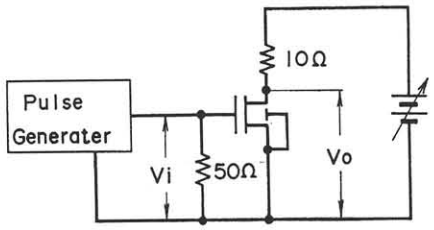
Fig.10. On-resistance characteristics.

Table II Comparison of three power MOSFET structures.

	Structure	Wgmax per unit area	Ideal Ron ratio *
New Type		$\frac{1}{C}$	1.0
VMOS		$\frac{1}{C+\sqrt{2}\,xjp}$	2.4
DMOS		$\frac{1}{C+2xjp}$	3.0



(a) Input / Output



(b)

Fig.11. (a) Input and output waveforms.
(b) mesuring circuits.

§5. Conclusion

The structure, design, and fabrication process of the vertical sidewall channel power MOSFET is demonstrated. The new power MOSFET is featured by the highest packing density and thereby the lowest on-resistance especially in the low breakdown voltage range.

Further reduction of the on-resistance on the same chip area is expected by applying finer design rule. The present new power MOSFET is attractive in respect for a variety of applications such as a synchronized rectifier and a semiconductor relay.

Acknowledgement

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