A High Performance, High Voltage Lateral pnp Transistor

Yoshitaka Sugawara and Tatsuya Kamei

Hitachi Research Laboratory and Takasaki Works, Hitachi, Ltd.

Hitachi and Takasaki, Japan

A new lateral transistor, the SADDL (Self-Aligned Double Diffused Lateral) transistor was developed for high voltage linear ICs. It has a self-aligned narrow n base to provide high h_{FE} and high f_T , and an electric field reducible p⁻ collector and electrodes to provide high BV_{CEO}.

It was confirmed that the SADDL transistor improved trade-off between $f_{\rm T}$ and BV_{CEO} by more than ten times that for other reported lateral transistors. A fabricated SADDL transistor of the 350 V class has a high $h_{\rm FE}$ (~100), high $f_{\rm T}$ (~15 MHz), and high Early voltage (>1000 V).

§1. Introduction

Recently, high voltage linear ICs, such as vertical deflection output ICs for color TVs and SLICs (Subscriber Line Interface Circuits) for time division exchange, have been developed. In these linear ICs, complementary npn and pnp

transistors are required.^{1,2,3)}

The lateral pnp transistor, shown in Figure 1(a), is widely used in linear ICs because of its process compatibility with a double diffused vertical npn transistor. But, in high voltage applications, it has a very poor performance because of its lightly doped base: to avoid punch-through between the emitter and the collector and to achieve a high breakdown voltage, a wide base width is required. This results in low current gain (h_{FE}) , low gain-This bandwidth product (f_T) and low Early voltage. To improve its poor performance, some modified lateral transistor structures have been developed, but the f_T value of these transistors are very low as compared with those of vertical npn $transistors.^{1,4,5)}$

On the other hand, utilizing vertical npn and pnp transistors has led to excellent performance in some devices $^{6,7)}$ but the fabricating processes are complex.

In this paper, in order to realize high device performance and a simple fabrication process, a lateral transistor with a new structure is presented.

§2. Device Structure

Figure 1(b) shows the cross-sectional view of the newly developed transistor, which is named SADDL (Self-Aligned Double Diffused Lateral) transistor. To achieve high h_{FE} and high f_T , a narrow n base is necessary like that in the vertical transistor. Therefore, by using the self-aligned technique, the p emitter (p_E) of the SADDL transistor is diffused from the same photo-etched SiO₂ hole that its n base (n_B) is diffused from. To implement the simple fabrication process, it is desirable to diffuse p_E simultaneously by the same boron diffusion process as for the p base of the vertical npn transistor.

To achieve high BV_{CEO}, the p⁻ layer (p_C^-) is utilized. Its surface impurity concentration (ND) is designed to be lower than n_B and higher than the n⁻ substrate. Since the p_C^- must act as the collector in the range of the operating voltage, p_C^- should not be completely depleted. But, when a high voltage, which is equal to the breakdown voltage is applied to the SADDL transistor, the depletion layer should be fully extended into p_C^- , but only slightly into n_B. Thus, punch-through between the emitter and the



(a) Conventional







(b) Calculation Model

Fig. 2. SADDL transistor fabricated by EPIC process and its calculation model. (The symbols O, □, △ indicate the site a, b and c, respectively.)

collector is avoided in spite of the narrow ng, and, at the same time, the electric field at the corner of the $p_{\rm C}$ - n⁻ junction is also reduced and high BV_{CEO} is achieved.

As an integration method for high voltage ICs, the EPIC (Epitaxial Passivated Integrated Circuit) method is superior to the pn junction isolation method because of the high isolation voltage, small isolation area and no latch up actions. Therefore, the SADDL transistor, which is fabricated in the dielectrically isolated island by EPIC method, is investigated.

In order to optimize the cross-sectional dimensions of the SADDL transistor, two dimensional numerical calculations of the electric field and the breakdown voltage have been used. Figure 2 shows the calculation model for the SADDL transistor fabricated by the EPIC process. The calculation method is almost the same with that developed in a previous paper.²⁾

Figure 3 shows the calculational relationships between the breakdown voltage and ND for the SADDL transistors with three kinds of $p_{\overline{C}}^{-}$ depth. When ND is much lower than each peak point of the curves, the breakdown voltage is limited to the small value by the electric field at site b shown in Figure 2(b), because the depleted layer extends into $p_{\overline{C}}^{-}$ more easily and is abruptly stopped at $p_{\overline{C}}^{-}$ When ND closely approaches the value of the peak points, the breakdown voltage becomes limited by the electric field at site a and becomes a large value. When ND is higher than that of the peak points, the breakdown voltage is limited by the electric field at site c and abruptly becomes small. By using Figure 3, ND can be optimized.

The other dimension parameters, such as the length of the electrodes and SiO_2 thickness under the electrodes, are also optimized by using the calculational results.



Fig. 3. Calculational relationships between breakdown voltage and surface impurity concentration of $p_{\rm C}^-$ layer, ND.



Fig. 4. Experimental relationships of BV_{CBO}, h_{FE} max and f_{T} max versus impurity concentration of $p_{\overline{C}}^{-}$ layer. The h_{FE} max and f_{T} max are rather low because the n_{B} impurity profiles of these samples are not yet optimized.

§3. Experimental Results

3.1 Dependence of electrical characteristics on ND

Figure 4 shows the experimental relationships of BV_{CBO} , $h_{FE}max$ and f_Tmax versus boron dose of p_C^- layer for the SADDL transistors fabricated by the EPIC method. Since h_{FE} and f_T depend on the collector current (Ic), their maximum values, $h_{FE}max$ and f_Tmax , are plotted in the figure. The curve of the collector-base breakdown voltage (BV_{CBO}) shows the good qualitative agreement with the calculation curve shown in Figure 3. The $h_{FE}max$ and f_Tmax



Fig. 5. Dependence of h_{FE} and f_T on I_C .

increase as the boron dose increases. The collector current (Icmax), for which h_{FE} and $f_{\rm T}$ begin to decrease abruptly, also increases in proportion to the increase in boron dose. The cause seems to be the reduction of the base spreading effect, $^{9)}$ which results from conductivity modulation in the $p_{\rm C}^-$, and the decrease in the collector resistance.

3.2 Dependence of electrical characteristics on Ic and $\ensuremath{\mathbb{V}_{CE}}$

Figure 5 shows the relationships between the electrical characteristics and Ic of the SADDL transistor. The area of the SADDL transistor is about 0.045mm^2 and its emitter area is about $1200 \mu \text{m}^2$. In order to reduce the transistor area, the field reduction region technique which was developed previously⁸⁾ is utilized. The n base impurity profile is controlled to achieve the higher hFE and fT than those of the transistors shown in Figure 4. The electrical characteristics of a conventional transistor with the same area are also shown in Figure 5, but its fT is so low, less than 0.5 MHz, that it is not indicated. The hFE and fT of the SADDL transistor are very high as compared with those of the conventional transistor. The current capacity is also increased.

Figure 6 shows the common emitter output characteristics of these transistors. In SADDL transistor, the dependence of Ic on V_{CE} is improved remarkably. The Early voltage is larger than 1000 V. This output characteristic is also important for high voltage linear ICs.

Figure 7 shows the dependence of $f_{\rm T}$ on the applied voltage, $V_{CE}.$ The $f_{\rm T}$ increases according to the increase in $V_{CE},$ but its dependence on V_{CE} is less than that of the improved conventional transistor, whose emitter is disposed close to the inclined n⁺ layer shown in Figure 2 in order to increase h_{FE} and $f_{\rm T}$ by utilizing the reflection effect of injected holes into the $n_{\rm B}^-$ base. $^{8)}$

3.3 Trade-off between f_T and BV_{CEO}

Generally, lateral transistors have the tendency that hFE and f_T become high, but BVCEO and BVCEO become low according to decreases in n base width. Figure 8 shows the trade-off between f_T and BVCEO for the three kinds of lateral transistors. The solid line and the dotted line show the trade-off for the SADDL



(a) Conventional







Fig. 7. Dependence of f_T on V_{CE} of lateral pnp transistors.

transistor and the conventional transistor, respectively. The broken line shows the trade-off



Fig. 8. Trade-off between fT and BVCEO for lateral pnp transistors.

for the transistor with the structure removed $\ensuremath{n_{\rm B}}$ from the SADDL transistor, namly, the structure only. To achieve high breakdown with $p_{\overline{c}}^-$ only. To achieve high breakdown voltage, the n⁻ base width of this transistor must be wide. It has been designed at 17.5 -47.5 μ m. This transistor with p_C^- only has a trade-off of the same level as that for other modified lateral transistors which have been reported. $^{1,4,5)}$ The trade-off for the SADDL transistor is improved about ten times over that for the transistor with p_{C}^{-} and about a hundred times over that for the conventional transistor.

\$4. Conclusion

A new lateral transistor, the SADDL (Self-Aligned Double Diffused Lateral) transistor was developed for high voltage linear ICs. It has a self-aligned narrow n base to provide high $h_{\rm FE}$ and high fT, and electric field reducible p collector and electrodes to provide high BVCEO. The structure was designed using a two dimensional numerical calculation method.

The fabricated SADDL transistor has high $h_{\rm FE}$ (~ 100), high $f_{\rm T}$ (~ 15 MHz) and high Early voltage (>1000 V) as compared with the conventional transistor with the same high BVCEO (~350 V). The SADDL transistor was able to improve trade-off between fT and BVCEO by about ten times that for the modified transistors and a hundred times that for the conventional transistors.

Such higher performance levels of the SADDL transistor allows its applications to high voltage linear ICs such as TV output circuits, SLICs for time division exchange and driver ICs for displays and motors.

Acknowledgements

The authors wish to thank Drs. T.Takasuna, M.Okamura and T.Kariya and Messrs. K.Miyata, K.Nagata and M.Kawanami for their continuous encouragements. Appreciation is also expressed to members of the IC Fabrication Group for their constant support.

References

- M.Kimura, M.Yoshimura and F. 1) I.Imaizumi, Inoue : IEEE Trans. on Consumer Electronics, CE-26, p.367, Aug., 1980. Y.Sugawara, T.Kamei and Y.Hosokawa : Proc.
- 2) 4th International Conf. on Solid State Devices, Tokyo, p.53, Aug., 1982; Japan. J. Appl. Phys. 22 (1983) Suppl. 22-1, p.77.
- 3) T.Ohno, T.Sakurai and Y.Inabe : ISSCC Digest of Technical Papers, p.230, Feb., 1984. J.D.Beason. : IEDM Technical Digest, p.424,
- 4) Dec., 1983.
- S.Krishna and A.Ramde : IEEE Journal of 5) vol.SC-17, p.781, Solid State Circuits, 1982.
- 6) T.Sakurai, K.Kato, Y.Inabe and T.Hayashi : IEDM Technical Digest, p.793, Dec., 1982.
- J.D.Beason : IEDM Technical Digest, p.89, 7) Dec., 1982.
- Μ. T.Kamei, Y.Hosokawa and 8) Y.Sugawara, IEDM Technical Digest, p.412, Okamura : Dec., 1983.
- C.T.Kirk : IRE Trans. on Electron Devices, 9) vol.ED-5, p.164, 1962.