

A High Resolution CCD Image Sensor Overlaid with an a-Si:H Photoconductive Layer

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A high resolution CCD image sensor, overlaid with an a-SiC:H(i)/a-Si:H(i)/a-SiC:H(p) photoconversion layer, has been fabricated. High level resolution features have realized by zig-zag pixel layout and novel interline transfer CCD, which can read out two horizontal rows simultaneously. A horizontal limiting resolution of 500 TV lines has been obtained without increasing the conventional 400(H) pixel number.

§1. Introduction

Recently, solid state image sensors, including CCD, MOS and CPD, have been markedly improved in regard to their imaging characteristics and fabrication technologies. Among these imagers, the CCD is superior to other imagers in sensitivity or signal to noise ratio. MOS and CPD had an advantage in regard to high resolution image reproduction techniques, such as zig-zag pixel layout and simultaneous read-out of two horizontal rows¹⁾.

So far, monolithic CCD imagers have difficulty in applying similar high resolution techniques successfully adopted to MOS and CPD, without decreasing the present pixel packing density.

On the other hand, "two-level(two-story)" solid state imagers overlaid with photoconductive layers have attracted various amounts of interest for their promising characteristics, such as high spectral sensitivity and low blooming^{2,3,4)}.

The authors had fabricated a two-level CCD image sensor, which consists of 2/3" 400(H) x 500 (V) interline transfer CCD (IT-CCD) as a solid state scanner and an a-Si:H/a-SiC:H film as a photoconversion layer⁵⁾. A new high resolution CCD image sensor, composed of a novel IT-CCD scanner and an a-SiC:H(i)/a-Si:H(i)/a-SiC:H(p) photoconversion layer was achieved. The high resolution feature comes from the zig-zag pixel layout and the simultaneous read-out of two rows. This paper presents device organization, structure,

fabrication and performance.

§2. Device organization

Figure 1 shows a device organization diagram. In this device, 395(H) x 490(V) effective pixels are arranged in zig-zag format. Each vertical CCD (V-CCD) was constructed with 500 transfer stages instead of the 250 transfer stages for a conventional CCD, and its channel runs straight in a vertical direction. A horizontal read-out register have two 395-stage CCDs arranged in parallel.

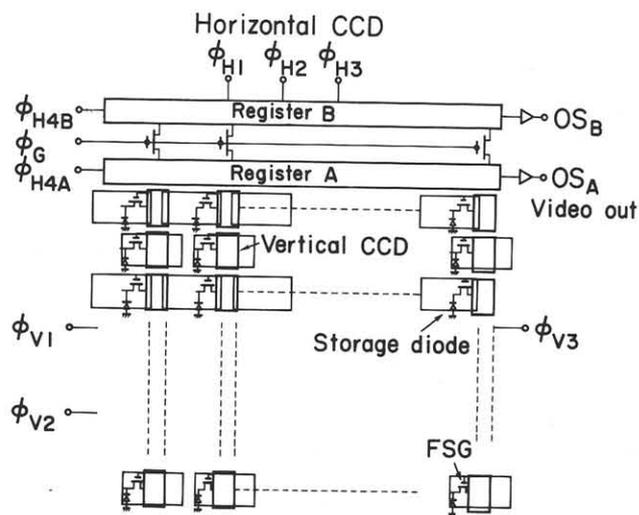


Fig. 1 Image sensor organization diagram.

By applying pulse voltages to a transfer gate (ϕ_G), the signal charge packets in two rows of the image area can be transferred to the double horizontal CCD registers. Figure 2 shows an SEM photomicrograph of the double horizontal CCD registers. By driving the double CCD registers at 7.16 MHz clock frequency, 790 signal charge packets in the two rows are read out at an equivalent frequency of 14.32 MHz, achieving simultaneous read-out of two rows. A row of 395 signals is interlaced with the next row of 395 signals and 790 signals rearranged in a row, resulting in high resolution being obtained.

§3. Device structure and fabrication

Figure 3 shows a cross sectional view of a unit cell. For a conventional 400(H) x 500(V) CCD, 250 V-CCD transfer stages are required. This number is equal to half of that for vertical pixels. For the new imager, 500 transfer stage V-CCDs were developed by employing a three layer poly-Si electrode structure driven in three phase operation. Thus, all signal charges for each pixel are read out every field time. The IT-CCD is fabricated on a p/p⁺ epitaxial wafer. The p-type layer has 5 $\Omega\cdot\text{cm}$ resistivity, and 10 μm thickness. The p⁺ substrate, whose resistivity is 0.05 $\Omega\cdot\text{cm}$, has a low life time for minority carrier diffusion. In order to decrease dark

current and image defects caused by CCD surface roughness, smoothing the CCD surface in contacts with the photoconductive layer was achieved successfully by using a polyimide film. After forming the first Al electrodes, the surface roughness on the CCD surface was 1.5 μm . By coating the polyimide film on the CCD surface, the CCD surface roughness was reduced to 0.2 μm . Then, the top of the first Al electrodes was surfaced by a uniform reactive ion etching of the polyimide layer. An electric connection between the first level Al and the second level Al is formed directly without any photolithography process.

Also, an intrinsic a-SiC:H film (50 \AA), an intrinsic a-Si:H (3 μm) and boron doped p-type a-SiC:H film (200 \AA) are continuously deposited on the IT-CCD scanner by glow discharge. The ITO (Indium-Tin-Oxide) electrode for applying voltages to the photoconductive films is formed on top of the p-type a-SiC:H film. The p-type a-Si:H film acts as a barrier to stop minority carrier (electron) injection from the ITO electrode. The thin intrinsic a-SiC:H film with high resistivity ($> 10^{13} \Omega\cdot\text{cm}$) formed between the intrinsic a-Si:H film and the CCD surface assures picture quality by keeping lateral leakage currents low on the polyimide surface.

As shown in Fig. 4, zig-zag pixel layout was designed by shifting the second Al electrodes a half cell pitch row by row. And a channel of V-CCD formed in the solid state scanner, runs

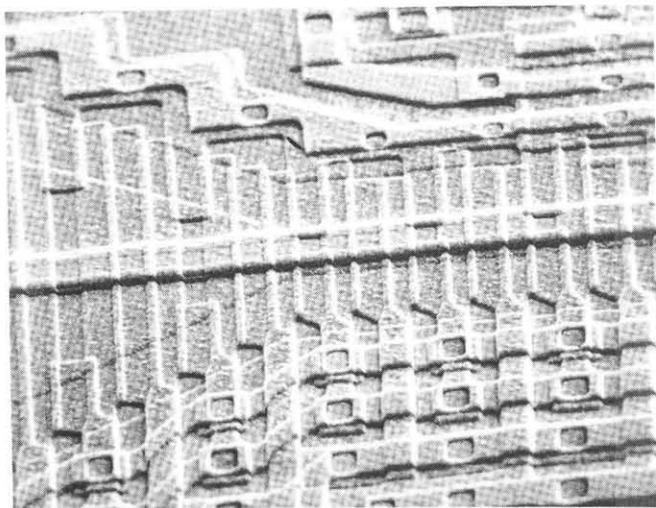


Fig. 2 Horizontal CCD SEM Photomicrograph.

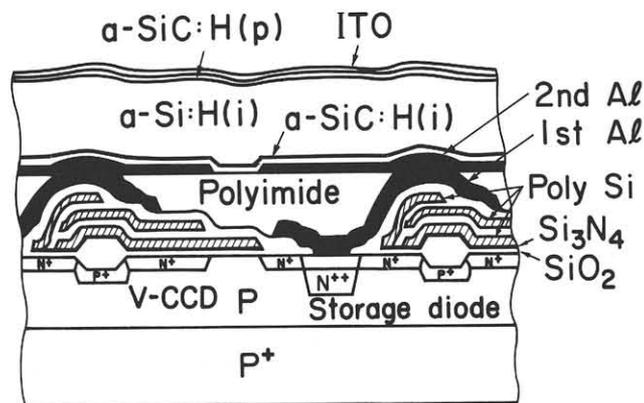


Fig. 3 A unit cell cross sectional view.

straight in a vertical direction as the conventional IT-CCDs.

Figure 5 shows a device surface SEM photomicrograph. In spite of the three layer poly-Si structure, the desired surface smoothing is realized. Unit cell size is $22\ \mu\text{m} \times 13\ \mu\text{m}$ and image area is $8.8(\text{H})\text{mm} \times 6.5(\text{V})\text{mm}$, which corresponds to 2/3" image format. Chip size is $9.9\ \text{mm} \times 7.7\ \text{mm}$.

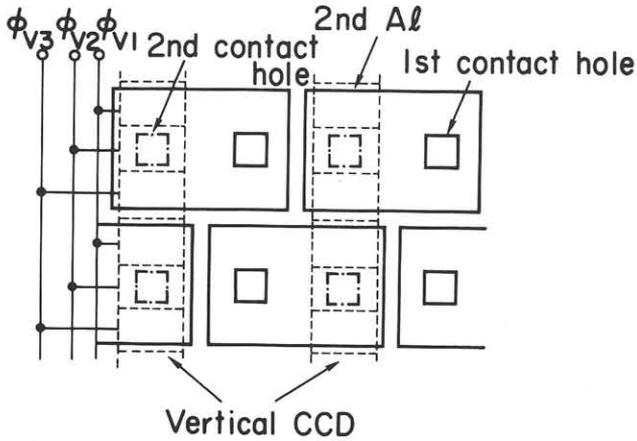


Fig. 4 Zig-zag pixel layout and three phase V-CCD.

§4. Performance

Figure 6 shows enlarged image pictures of RETMA resolution chart. The upper half of the image picture was taken by this new tow-level CCD imager. The lower half was taken by an ordinary two-level CCD imager. Horizontal limiting resolution is 500 TV lines, which is two times higher than that for a conventional pixel layout $400(\text{H}) \times 500(\text{V})$ CCD imager. Vertical limiting resolution of 400 TV lines are also obtained.

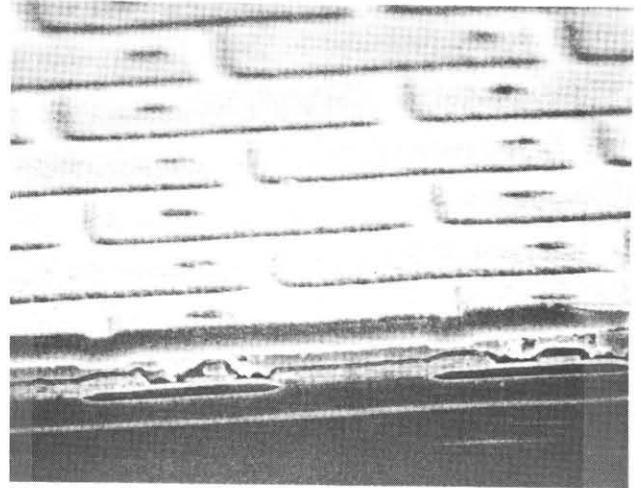


Fig. 5 Device SEM Photomicrograph.

Taken by new high resolution CCD image sensor.

Taken by conventional two-level CCD image sensor.

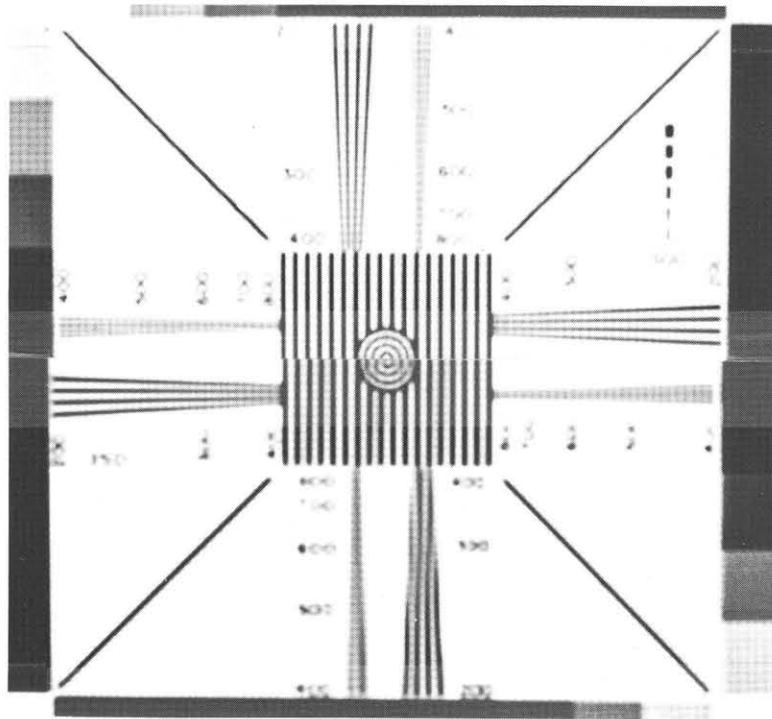


Fig. 6 Enlarged image pictures of RETMA resolution chart, taken by new high resolution CCD imager and taken by conventional $400(\text{H}) \times 500(\text{V})$ two-level CCD imager.

Sensitivity, dark current and lag were $0.14 \mu\text{A/lx}$, 1.5 nA and 5% at the third field, respectively. These results were same as those for a usual two-level CCD imager⁵⁾ fabricated simultaneously.

A larger photosensitive aperture, one of two-level CCD imagers features, suppressed moiré effect to a low value when compared with the zig-zag layout monolithic MOS or CPD. The device specification and performance are shown in Table 1.

§5. Conclusion

A two-level CCD imager with zig-zag pixel layout and simultaneous readout of two rows has been fabricated successfully without increasing pixel number and chip size. 500 TV lines horizontal limiting resolution and $0.14 \mu\text{A/lx}$ photosensitivity were obtained. This two-level CCD imager, with high resolution, high photosensitivity and low smear, is expected to be used as a second generation solid state imager.

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Number of pixels	395(H) x 490(V) (zig-zag layout)
Image area	8.8(H) x 6.5(V) mm ² (2/3" format)
Pixel size	22(H) x 13(V) μm ²
Chip size	9.9(H) x 7.7(V) mm ²
Sensitivity	0.14 μA/lx
Saturation signal	200 nA
Dark current	1.5 nA
Image smear	< 0.01 %
Limiting resolution	
Horizontal	500 TV lines
Vertical	400 TV lines

Table 1. Image sensor specification and performance

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