

A Color CCD Image Sensor for Imaging Photographic Negatives

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A charge-coupled color image sensor with 740(H) x 484(V) resolution elements is described. The sensor is for imaging color photographic negatives, and the sensor outputs are used for reconstructing the positive-image NTSC video signal. The negative-to-positive reversal process has imposed many unique requirements. The sensor achieves charge capacity of 800,000 electrons per pixel, random noise of 150 electrons per pixel, and dynamic range of 74 dB. Sensor design, spectral sensitivity, charge capacity, and noise are discussed.

Introduction

The imaging of color photographic negatives poses many unique requirements for solid-state image sensors which are not normally encountered by sensors for direct scenes. In a photographic negative, the highlight of the scene becomes the darkest area of the negative. Therefore, a very wide dynamic range is required for the conversion from negative to positive. High blue sensitivity is required for compensating the short-wavelength absorption in the film base. High pixel counts are desirable to minimize aliasing. We have designed and fabricated a single-chip, 2/3" format, color CCD imager for this purpose. The sensor has 740 H x 242 V imaging pixels, which gives 740 x 484 resolution elements by the standard interlacing method.

Sensor Design

The sensor architecture is shown in Figure 1. The sensor consists of a four-phase CCD image area, dual two-phase horizontal registers, and separate output amplifiers for each of the three colors. During the vertical retrace interval the photographic negative is illuminated. The vertical clocks are held constant to integrate the signal charge. At the end of the vertical retrace interval the signal charge is read out. A row at a time is transferred into the horizontal registers. The charge from columns with green color filters is transferred to the top register while the charge from the alternate columns with red

and blue color filters is transferred to the bottom register. The dual horizontal register design was required to achieve the 12 μm horizontal column spacing without a third level of polysilicon. The horizontal registers are read out at a 7.16 MHz pixel rate. The charge is sensed by floating diffusion outputs and buffered by dual-stage buried-channel source followers. The image area is 8.88 mm(H) x 6.58 mm(V). The channel-stop region is 2 μm wide, and the buried channel is 10 μm wide. The gate oxide under both the first and second polysilicon electrodes was 1600 \AA thick, and the polysilicon layers were both ~ 1700 \AA thick, to maximize optical transmission in the blue.

Spectral Response

In a color image sensor in which the photosensitive area is fully covered by polysilicon, careful choice of polysilicon thickness is required to achieve adequate transmission in the blue while maintaining sufficiently low resistance to transfer charge vertically. The absorption coefficients of the polycrystalline silicon vary with phosphorus concentration (1). The more heavily doped polysilicon we used displays lower absorption in the visible. We attribute this to enhanced grain growth during oxidation due to the higher phosphorus concentrations. The spectral response of the sensor is shown in Figure 2. At wavelengths below 500 nm the response is dominated by optical absorption in the poly-

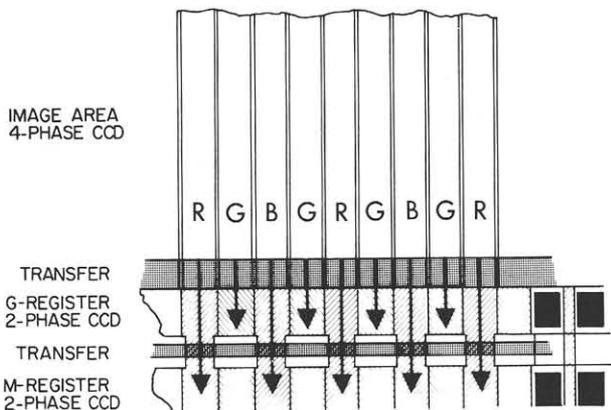


Fig. 1. Design of image sensor. Sensor has 740 columns horizontally with R-G-B-G stripe color filter pattern. Vertical registers are four-phase CCD's; horizontal registers are two-phase.

silicon electrodes. Between 500 and 800 nm the response is dominated by structure due to optical interference within the polysilicon and the gate oxide. Beyond 800 nm the light is absorbed well below the silicon surface, and the spectral response decreases owing to recombination of the photogenerated electrons. Figure 2 also shows quantum efficiency calculated using the complex optical constants for oxide and doped polysilicon and the independently measured thicknesses of gate oxide, polysilicon, and the overlying oxide. The minority-carrier diffusion length was used to fit the decrease in response in the infrared. The optical transmission was calculated by the matrix method using fresnel coefficients. Peak response at 450 nm requires a gate oxide thickness of 1600 Å. Because of the decrease in charge capacity with gate oxide thickness, a compromise is required between charge capacity and blue sensitivity in these devices.

Organic color filter arrays are fabricated on top of the sensor in a R-G-B-G stripe geometry.

Charge Capacity

Because of the large density range of photographic negatives, a wide dynamic range is required in the sensor. There are two limitations to charge capacity in a buried-channel CCD: (1) the interaction between electrons and interface states at the Si-SiO₂ surface and (2) the potential difference between well and barrier electrodes. Figure 3a illustrates the first limitation.

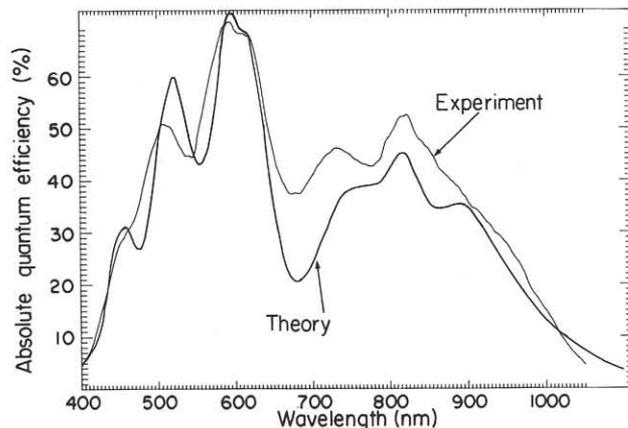


Fig. 2. Measured and calculated spectral response of sensor.

The potential and the electron distribution were calculated by solution of Poisson's equation in one dimension using Hermite Orthogonal Collocation (2). Majority and minority carriers were taken into account in a self-consistent fashion. The dopant distribution in the buried channel was obtained using the SUPREM process-modeling program. Results for a buried-channel phosphorus dose of $1 \times 10^{12} \text{ cm}^{-2}$ are shown. As more electrons are added to the channel, the barrier to the surface decreases. Capture of electrons at interface states can occur when the vertical transfer time T_{tr} is longer than the capture time constant $\tau_c = 1/\sigma v n_s$, where σ is the interface state cross-section, v is the thermal velocity, and n_s is the surface electron density. The surface electron density can be related to the peak density of electrons in the channel n_{CH} and the channel potential ϕ_c :

$$T_{tr} > \tau_c = 1/\sigma v n_s = \frac{1}{\sigma v n_{CH}} \exp \left[\frac{(\phi_s - \phi_{CH})}{KT} \right] \quad (1)$$

For buried-channel doses in the range of $1-2 \times 10^{12} \text{ cm}^{-2}$, $n_{CH} \approx 3 \times 10^{16} \text{ cm}^{-2}$. Capture of channel electrons by the surface state thus occurs when the barrier to the surface is less than 300 mV. The relationship between the number of electrons per pixel and the barrier to the surface is shown in Figure 3b. For the $1 \times 10^{12} \text{ cm}^{-2}$ buried-channel dose, the calculated charge capacity in the buried channel is 440,000 electrons per pixel. For a $2 \times 10^{12} \text{ cm}^{-2}$ dose, it is

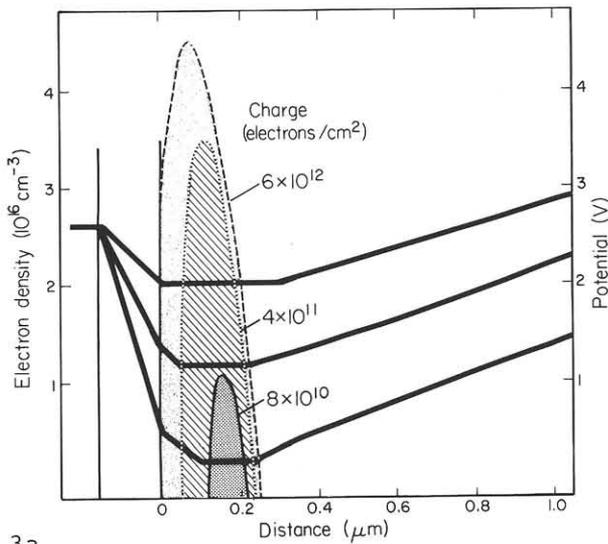
1,200,000 electrons per pixel.

Owing to the narrow channel width, two-dimensional effects significantly reduce charge capacity. The electrostatic potential and electron distribution in two dimensions is calculated using finite-difference techniques. At the transition between buried- and surface-channel operation ($\phi_{CH} - \phi_S = 300$ mV) for a 1×10^{12} cm⁻² buried-channel dose, the electrons occupy only the center 4 μ m of the 10 μ m channel. For a 2×10^{12} cm⁻² buried channel dose with a signifi-

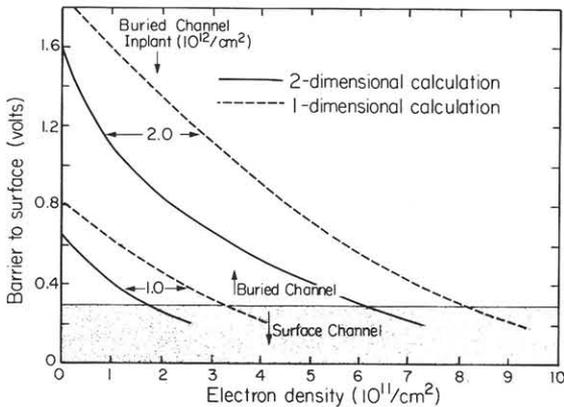
cantly larger barrier between channel and surface, the electrons occupy the center 7 μ m of the 10 μ m channel. Figure 3b shows the electron density in two dimensions for both buried-channel doses. From experimental measurement, the 1×10^{12} cm⁻² dose yields 100,000 electrons per pixel capacity, and the 2×10^{12} cm⁻² dose yields 800,000 electrons capacity, in good agreement with the two-dimensional model.

Horizontal Registers

The horizontal CCD registers, which matched the imaging area columns, have a pitch of 12 μ m for each of the two phases. We used 10 μ m for each first poly storage gate and 2 μ m for each second poly transfer gate. The signal charge corresponding to the red and blue columns is transferred through the top register storage area, through a transfer gate, then to the bottom register. The transfer region is bounded by channel stops on both sides, forcing the charge to "neck down" from a 10- μ m-wide region in the top register storage area to a narrower region between the two registers, as shown in Figure 1. In that narrower region under the same poly gate, the fringe fields from the channel stop reach all the way to the center of the channel, resulting in a smaller potential than under the normal gate area. Thus the effect of "necking down" is a barrier to charge transfer from the 10- μ m-wide gate in the top register into the narrower transfer region. A two-dimensional electrostatic potential calculation has been carried out for the separation of the channel stops at 8, 6, and 4 μ m of channel width. The calculated barrier height is shown in Figure 4 as a function of the channel potential of the storage gate. The barrier height is measured on a test device having 8 μ m mask width; the measured data points are the triangles in Figure 4. The amount of charge retained by the barrier will be dependent on the size of the top register and the clock voltages. If the barrier height were uniform across the whole length of the horizontal register, then a constant amount of charge would be retained in the top register, causing a zero shift in the output signal. However, the barrier height is not a constant, owing to the variation in the substrate as well as the fabrication processes. The varia-



3a



3b

Fig. 3. (a) Electrostatic potential and electron distribution for different quantities of charge in the buried channel.

(b) Potential barrier between buried channel and surface as a function of electron concentration for two buried-channel doses. Results of one- and two-dimensional models are shown.

tion of barrier height will result in a fixed pattern in a complementary manner for the top and bottom registers. The above-described barrier can be avoided by widening the distance between channel stops at the transfer region and by transferring out the last few electrons at the lowest possible channel potential of that storage gate. By doing so, we have circumvented that barrier problem.

Noise

The noise sources in this sensor include pattern and shot noise from dark current, output amplifier noise, and photosensitivity pattern noise due to the sensor and the color filter array.

The dark current in better sensors at room temperature was 3 nA/cm^2 or 900 electrons per pixel, causing 30 rms electrons of shot noise and 60 rms electrons of pattern noise.

The largest random noise source is the output amplifier at 120 rms electrons per pixel in a 3.5 MHz bandwidth. The output amplifiers are two-stage buried-channel source followers with sensitivity of $2 \text{ } \mu\text{V/electron}$. Owing to the use of buried-channel transistors and to double correlated sampling in the signal processing, the output amplifier noise is almost entirely a result of thermal noise in these transistors.

Photosensitivity pattern noise is caused by pixel-to-pixel variations in photosensitive area and transmission variations of the overlying device layers and the color filter array. The rms photosensitivity pattern noise values in sensors without color filters range from 0.5% to 1.2% of the signal. This value is largely independent of wavelength throughout most of the visible. The color-filter pattern noise, however, is strongly wavelength dependent, varying with changes in the illuminant and with sensor spectral sensitivity. Measurements of an integral color filter on an imager yielded an overall pattern noise of 1.4%.

The signal and the noise from various sources are plotted as a function of negative density in Figure 5. The dynamic range of the sensor is 74 dB. This exceeds the dynamic range required for imaging photographic negatives.

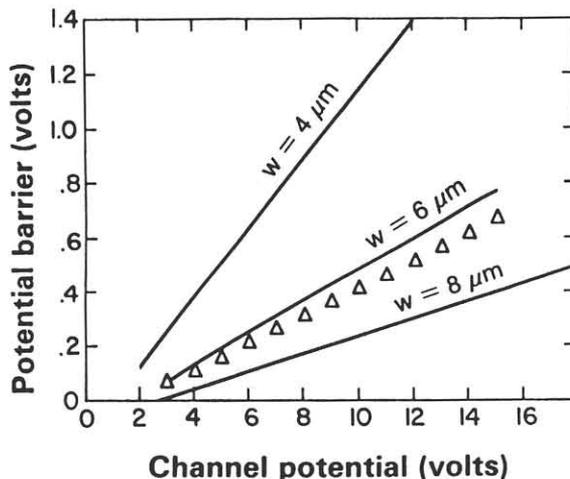


Fig. 4. Potential barrier at the "neck-down" region as a function of the normal channel potential for 3 different channel widths. The triangles are the measured barrier for a test device of $8 \text{ } \mu\text{m}$ mask width.

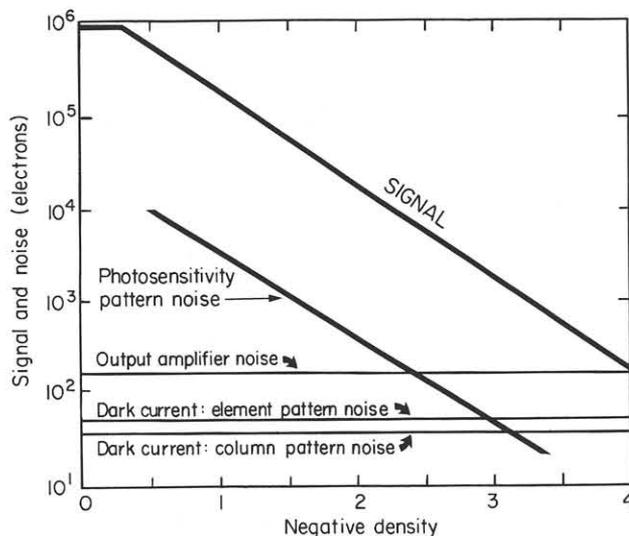


Fig. 5. Signal and noise as a function of the density of the photographic negative. Dynamic range of the sensor is 74 dB.

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