

A CCD Imager on Three Types of P-Wells

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A 488x590-element CCD imager for the 2/3" format employing three types of p-wells has been developed and was found to exhibit very small smearing as well as complete blooming suppression. For 10-percent vertical height illumination, the smear signal was -73dB of the illumination signal (550nm). Furthermore this imager employs n^+-n^-p photodiodes to reduce the change of spectral response with the storage of signal charge.

§1. INTRODUCTION

The performance of solid-state imagers has continued to improve. With the development of VLSI technology, blooming control in CCD imaging devices with television resolution has been realized by incorporating diffused bus drain lines (1). Another approach that employs a vertical overflow drain (2) has also been accomplished. But smearing has not been suppressed enough in contrast with the fact that electron-beam-scanned camera tubes do not suffer from such phenomenon. In terms of interline-transfer CCD imagers, the diffusion of photogenerated carriers to neighboring shift registers causes vertical smearing. To reduce the smear signal, a scheme which adds a frame storage area to an interline-transfer organization was investigated (3). But this organization requires a chip size of almost twice.

This paper will describe a CCD imager with a new structure that reduces the smear signal. The CCD shift registers in this imager are located in a p-well that is made shallow enough so as to be fully depleted and to prevent the diffusion of photo-generated carriers to them. In addition, this imager utilizes n^+-n^-p photodiodes instead of n^+-p diodes. Owing to the introduction of n^- -region, the change of spectral response in accordance with the amount of stored signal charge is alleviated.

§2. DEVICE STRUCTURE

The sensor is organized in an array of 488 hor-

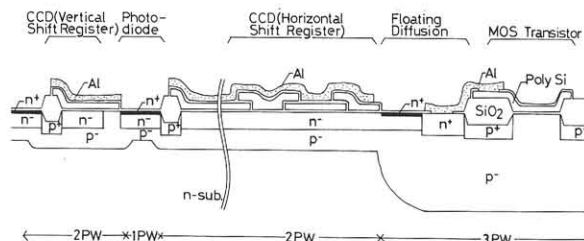


Fig.1. Cross-sectional view of the imager.

izontal lines by 590 vertical columns, 20 columns out of which are fully opaqued by a topside layer of aluminum to provide a black reference. The photoelement pitch is 15 μ m horizontally and 13 μ m vertically. The device utilizes an interline-transfer scheme. The vertical shift registers consist of 4-phase buried-channel CCD's. On the other hand, the horizontal shift register consists of a 2-phase buried-channel CCD with ion implanted barriers. The imaging area of the device is 8.55mm x 6.37mm, corresponding to the 2/3" optical format. The chip size is 10.0mm x 8.4mm.

Fig.1 shows a cross-sectional view of the imager including a unit cell, the horizontal shift register and the output amplifier. Each photocell consists of one n^+-n^-p photodiode and a half stage of the vertical shift register. The device employs two levels of polysilicon layer and three types of p-wells instead of two (2). The photodiode is located in a lightly doped shallow p-well (1PW), and the vertical and horizontal shift registers are made in a slightly deeper p-well (2PW). Their depths are 1.2 μ m and 1.8 μ m, respectively. On the

other hand, MOS transistors which make up the output amplifier are fabricated in a deep p-well (3PW). The n-type substrate is reverse-biased with respect to the p-wells. The 1PW is depleted to transfer the excess photogenerated carriers to the substrate. The 2PW is also completely depleted so as to prevent the photogenerated carriers from diffusing to neighboring CCD vertical shift registers. It should also be pointed out that this shallow p-well structure make it easy to shrink the cell size owing to the small lateral diffusion of the dopant.

§3. DEVICE OPERATION

The clock pulses for the vertical shift registers are shown in Fig.2. The ϕ_{V1} and ϕ_{V3} clocks drive the gates which are comprised of the upper level polysilicon layer and switch between three voltage levels-- V_L (low), V_I (intermediate), and V_H (high). On the other hand, the ϕ_{V2} and ϕ_{V4} clocks are fed to the gates which are comprised of the lower level polysilicon layer and switch between two voltage levels-- V_L and V_I . At the beginning of the readout of an even field, charge packets in the even-numbered photodiodes are transferred to the vertical shift registers via the surface-channel potential barriers by holding the ϕ_{V1} clock at V_H (4), while charge packets in the odd-numbered photodiodes are kept back by the surrounding electrodes biased at V_L or V_I (5). Fig.3 depicts potential profiles under the photodiode when its potential is reset to the surface-channel potential underneath the ϕ_{V1} electrode (EMPTY), and when excess carriers generated by optical overloads flow into the substrate suppressing blooming (FULL). As photogenerated signal charge is integrated in the photodiode, its potential decreases and the position of potential minimum (x_p) nears the n⁻-region and finally reaches there when all the photogenerated charge is transferred to the substrate. Since the carriers generated from that point to the surface are stored, the spectral response changes as the amount of stored charge increases. And the spectral response at short wavelengths in the n⁺-region is limited due to heavy recombination of the photogenerated carriers. But it should be noticed that this imager employs an n⁺-n⁻-p-n structure instead of an n⁺-p-n structure. This new structure reduces the change of the spectral

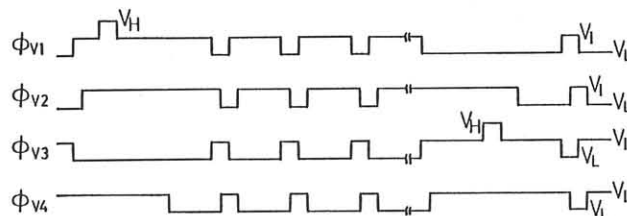


Fig.2. Operating pulse waveforms for the vertical shift register.

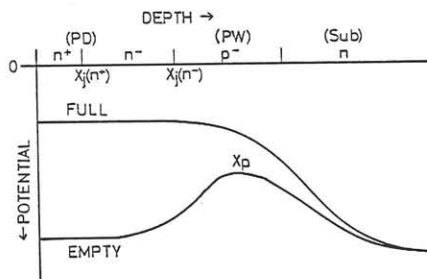


Fig.3. Potential profiles of the photodiode.

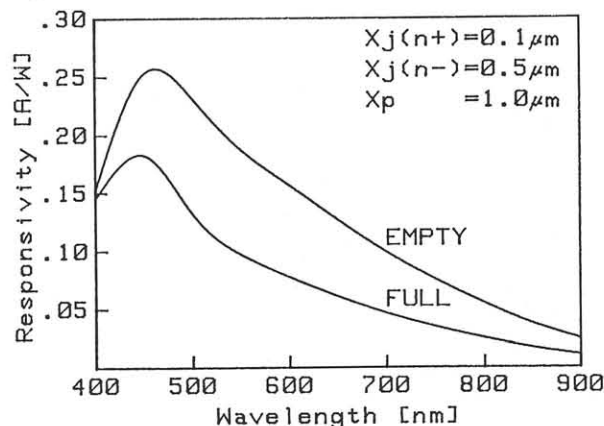


Fig.4. Calculated responsivity of an n⁺-n⁻-p-n structure.

response owing to the introduction of n⁻-region, which was originally proposed by Chamberlain to improve the blue response of n⁺-p photodiodes (6). When all the photogenerated charge is transferred to the substrate, the position of potential minimum reaches the n⁻-region. But the spectral response at short wavelengths is not limited due to its low impurity concentration. Fig.4 shows an example of calculated responsivity under the assumption that all carriers generated within the region mentioned above are collected as a result of the high field and that there is essentially no recombination within this region (7). And the n⁺-region is regarded as a dead layer. It should be noticed that responsivity still exists even when the photodiode is 'full'.

§4. DEVICE CHARACTERISTICS

4.1 Operating Condition

As the CCD shift registers are located in a de-

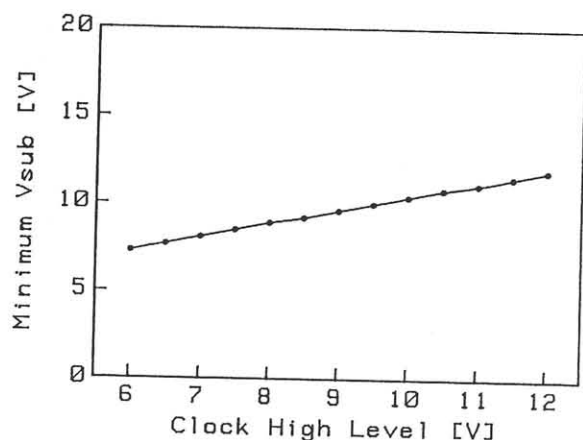


Fig.5. Minimum V_{SUB} dependence on clock high level.

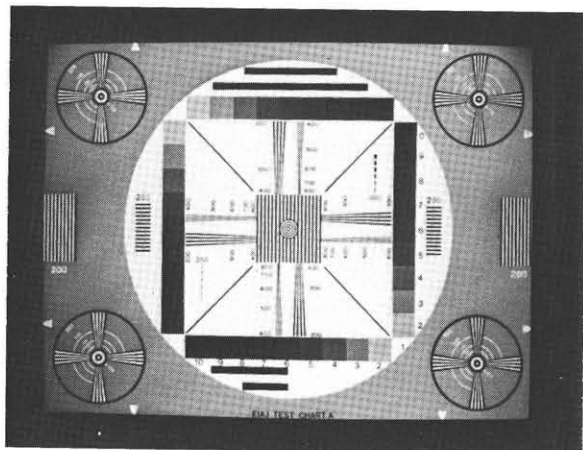


Fig.6. Imagery of a ITE resolution chart.

pleted p-well (8)(9), the lower limit of V_{SUB} (substrate bias voltage relative to the grounded 3PW) is determined by the operating condition of the CCD shift registers. Electrons are injected from the substrate to buried-channel CCD's when V_{SUB} is too low. Fig.5 shows the experimentally obtained relation between minimum V_{SUB} , below which carriers are injected, and CCD shift register clock high level. It is seen that the former increases as the latter increases and that this device requires to be operated at a V_{SUB} above 10V when CCD shift register clock high level is 9V.

4.2 Resolution

Fig.6 represents a television display of a ITE resolution chart. The horizontal and vertical resolutions are 420 TV lines and 480 TV lines, respectively. These are the maximum values expected from the number of the photoelements.

4.3 Saturation Current

Results of saturation current measurements are shown in Fig.7. In these measurements V_I was held at 0V to bias the surface-channel region into accumulation, while V_L was held at -4.5V to obtain max-

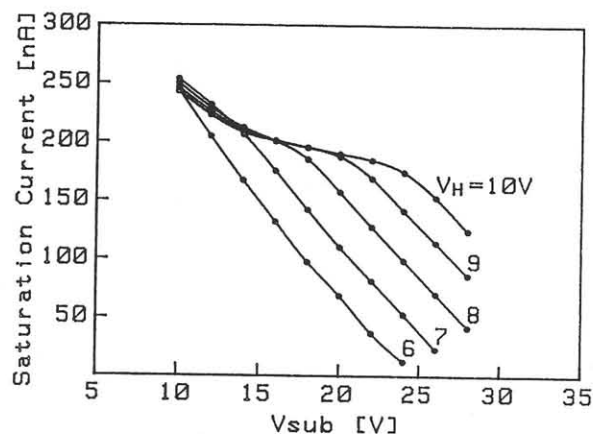


Fig.7. Saturation current versus substrate voltage.

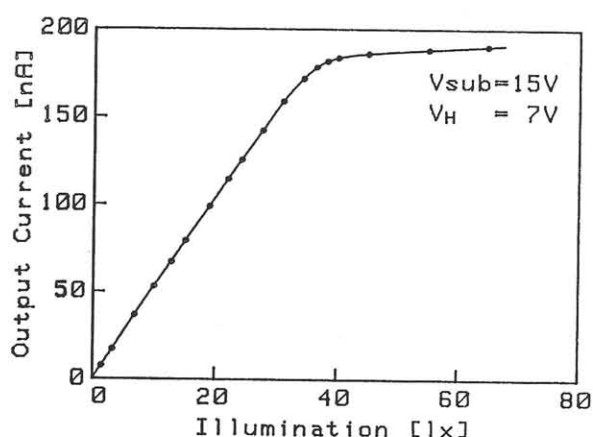


Fig.8. Photosensitivity to a 3100K halogen lamp. imum charge handling capacity of the vertical shift registers. Saturation current increases as V_H increases, but decreases as V_{SUB} increases. That is due to the fact that the charge handling capacity of the photodiodes increases as V_H increases or V_{SUB} decreases.

The photosensitivity of the imager with a 1mm-thick C-500 IR filter to a 3100K halogen lamp is shown in Fig.8. This characteristic represents a knee effect toward its saturation, which is favorable for use to video cameras.

4.4 Smear Characteristics

Fig.9 represents a reproduced image in the presence of a very intense optical overload by a 100W tungsten lamp. Fig.10 shows the ratio of the smear signal to the total signal for 10-percent vertical height illumination. The smear signal is as small as -84dB of the illumination signal at a wavelength of 450nm. Even at a wavelength of 550nm, to which the human eye is most sensitive, it is as small as -73dB. This very small smearing was obtained owing to the shallow p-well that incorporates the vertical shift registers.

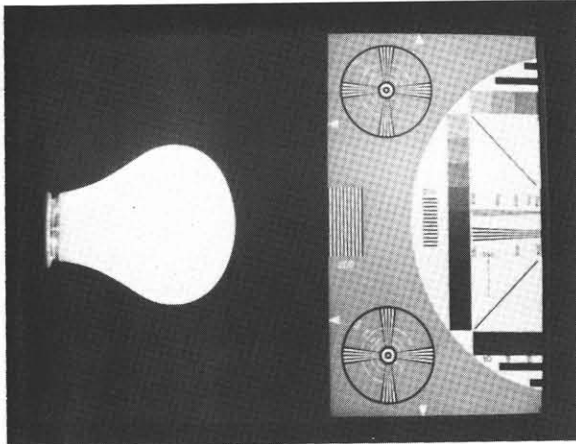


Fig.9. Imagery in the presence of a 100W tungsten lamp.

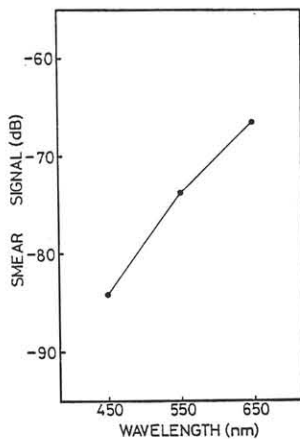


Fig.10. Smear signal as a function of wavelength.

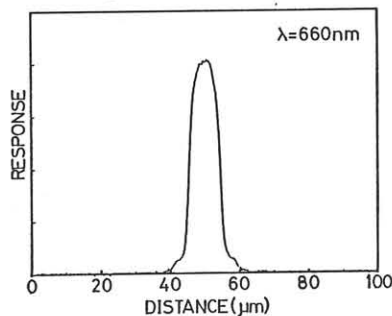


Fig.11. Response to a scanning 2μm-width illumination slit.

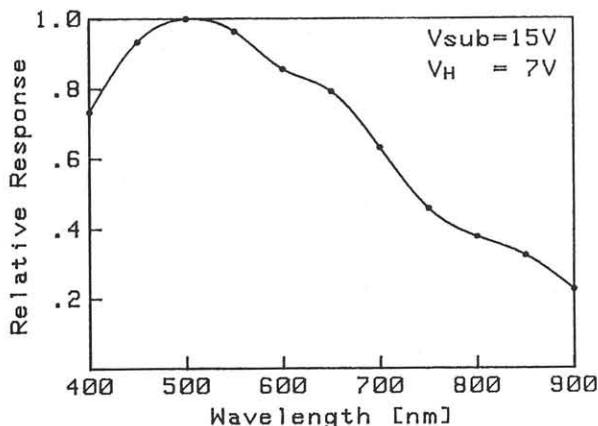


Fig.12. Spectral response of the device.

Fig.11 represents a response to a 2μm-width illumination slit which scans in the vertical direction. This result indicates very high vertical spatial resolution, as well as very high horizontal resolution that is evident from its very small smearing.

4.5 Spectral Response

The spectral response of the device is shown in Fig.12.

5. CONCLUSION

A 488x590-element CCD imager for the 2/3" format, which employs three types of p-wells and $n^+ - n^- - p$ photodiodes, has been described. It has been demonstrated that the shallow p-well structure offers a significant advantage in reducing the smear signal, as well as in increasing the spatial resolution. It has also been shown that the $n^+ - n^- - p - n$ structure alleviates the change of spectral response in accordance with the amount of stored signal charge. We are convinced that these structures will continue to be viable to provide high packing density devices with a shrunk chip size or with higher spatial resolution.

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