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Noise Modeling of New MOS Imaging Device Using Random Noise Suppression (RANS) Circuits

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Noise in random noise suppression (RANS) circuits has been analyzed on the basis of a time-domain noise analysis method. The RANS circuits suppress KTC noise, which has up to now been a limitation to the sensitivity of conventional MOS imaging devices. The dominant RANS noise source is seen to be 1/f noise from the driver transistor. This noise may be reduced by ensuring a large gate area and thin gate oxide thickness. Total noise for the new imager is as low as 0.7 nArms, which is 1/3 of the noise for a conventional MOS device.

1. INTRODUCTION

Single chip color MOS imaging devices[2] offer several advantages, when compared to interline-CCD imaging devices. These include no image lag, low aliasing, high resolution and high productivity. But, MOS device sensitivity, that is the signal to noise ratio, is expected to be further improved.

Accordingly, a new MOS imaging device has been proposed[3]. In it, X-Y arrayed photodiodes with MOS switches are combined with a horizontal bulk charge-transfer device (BCD) through random noise suppression (RANS) circuits. The key feature of the device is these RANS circuits. The circuits suppress KTC switching noise, and realize high sensitivity.

This paper presents an analysis of RANS circuit noise, and makes the RANS cirucuit noise suppression mechanism clear. Noise here is calculated on the basis of a time-domain noise analysis method[1]. 1/f noise, which has been neglected in analyses up to now, is also, in addition to thermal noise, cosidered as a noise source.

2. DEVICE STRUCTURE

A circuit diagram of the new imager is shown in Fig. 1. In this circuits, A and B signals are read into the 3-phase BCD during a blanking period, and simultaneously transferred through the BCD at a 14MHz rate in a double transfer operation during the scanning period. In the other field, the B and C signals are simultaneously picked up and interlaced to prevent image lag and aliasing.

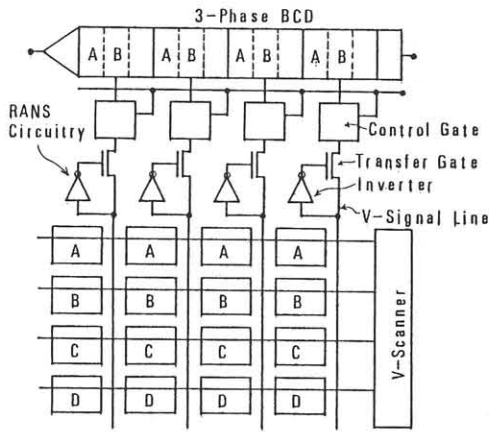

Fig. 1 Cirucuit diagram of MOS device with RANS circuits

The RANS circuits ensure high transfer effeciency from the vertical signal lines to the BCD. These high effeciency leads to high resolution, low color crosstalk and high smear suppression. In the RANS cirucuit shown in Fig. 2, the potential change of the vertical signal line due to signal transfer is amplified by the inverter, and fedback to the transfer gate. As a result, a charge can be transferred more rapidly from the vertical signal line to the BCD than with a conventional circuit.

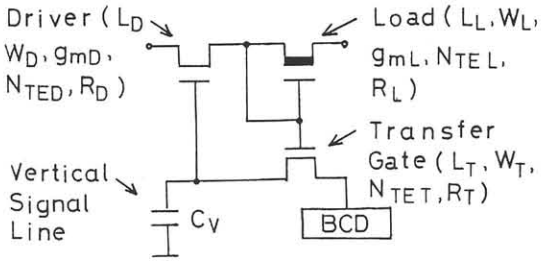

Fig. 2 RANS circuit

3. THEORETICAL ANALYSIS

Noise for the RANS circuit was calculated using a time-domain noise analysis method[1]. 1/f noise, which has been neglected in former analyses, was also considered as a noise source. The following two assumptions were made : 1) transfer gate was operating in a weak inversion region, and 2) the charge transfer loss was negligible.

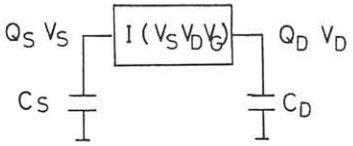

Fig. 3 Lumped model of charge transfer

A basic lumped charge model for the charge transfer is shown in Fig. 3. Charge, Q_S, stored on the capacitor, C_S, is transferred to the capacitor, C_D, through the conductance $I=I(V_S,V_D,V_G)$, where V_G is the gate voltage. With application of a time-domain noise analsis to this model, the mean-square fluctuation in the transferred charge $<q_D(t)^2>$ can be given as

$$<q_D(t)^2>=\int_0^t dt1\int_0^t dt2\ \exp\left(\int_{t1}^{t}\frac{dt1'}{\tau(t1')}\right)*\exp\left(\int_{t1}^{t}\frac{dt2'}{\tau(t1')}\right)\frac{\partial I}{\partial V_G}\bigg|_{t=t1}\frac{\partial I}{\partial V_G}\bigg|_{t=t2}<v_n(t1)v_n(t2)>(1)$$

Here, t is the time at the end of the transfer, v_n is the fluctuation of the gate voltage, and the time-dependent relaxation time is

$$\frac{1}{\tau}=\frac{1}{C_S}\frac{\partial I}{\partial V_S}\quad\text{----------(2)}$$

Thus, to determine $<q_D(t)^2>$, we must caluculate : 1) the time dependent quantities characteristic as derived from detailed (but noiseless) charge transfer solutions, and 2) the autocorrelation function of v_n.

A. Time-Dependent Quantities

When a transfer gate is operating in a weak inversion region, conductance, I, depends on an exponential form of V_G-V_S. With the RANS circuit, the change in voltage of the vertical signal line, V_S, is amplified by the inverter which has gain -G, and fedback to the voltage of the transfer gate, V_G. Under these conditons, we may solve noiseless charge transfer equation for I and obtain

$$\exp\left(\int_{t'}^{t}\frac{dt''}{\tau(t'')}\right)=\frac{At'+B}{At+B}\quad\text{----------(3)}$$

$$\frac{\partial I}{\partial V_G}\bigg|_{t=t'}=\frac{AC_V}{G+1}\frac{1}{At'+B}\quad\text{----------(4)}$$

where A and B are constant, and C_V is the parasitic capacitor of the vertical signal line.

B. Autocorrelation Functions

Each of the three MOS transistors of the RANS circuit shown in Fig. 2 generate both thermal and 1/f noise. The fluctuation of the gate voltage here stems from these six noise sources. Only noises with a driver transistor are amplified by the inverter.

Using the Wienner-kintchen theorem, we may gain the autocorrelation function from the power spectrum density of the fluctuation of the gate voltage. For example, the autocorrelation 1/f noise with a driver transistor can be expressed by

$$<v_{Df}(t1)v_{Df}(t2)>=G^2\int_0^\infty e_{Df}{}^2\cos 2\pi f(t1-t2)df.\text{-(5)}$$

Here e_{Df} is the input equivalent noise power spectrum density for the 1/f noise[4] of the driver transistor. Equation (5) can then be reexpressed as

$$<V_{Df}(t1)V_{Df}(t2)>=\frac{G^2q^2t_{ox,D}{}^2N_{TE,D}}{\mathcal{E}_{ox}{}^2L_DW_D}*\frac{\pi(2\pi|t2-t1|)^{R_D-1}}{2\Gamma(R_D)\cos(R_D\pi/2)}\quad\text{--(6)}$$

where q is the unit charge, $t_{ox,D}$ the gate oxide thickness, $N_{TE,D}$ the effective trap density, $\mathcal{E}_{ox}$ the dielectric constant, R_D the inclination of the 1/f noise power spectrum, and Γ a gammma function.

C. Noise Charge

We can simplify the equations for the mean-square fluctuations in the transferred charge by utilizing the assumption that charge transfer loss ξ is very small. Charge transfer loss, ξ, can be given by

$$\xi = \frac{\partial V_S}{\partial V_I} = \frac{B}{At+B} \quad \text{----------(7)}$$

where V_I is the initial voltage of the vertical signal line. By substituting Eqs. (3), (4) and the autocorrelation function into Eq. (1), we can then the noise expressions listed in Table 1.

This table indicates two significant results.

1) Noise from the transfer gate and load transistor, including in it kTC noise, reduced by the inverter. This is because the fast charge transfer capability of the RANS circuit reduces the effective capacitance of the vertical signal lines by a factor of 1/(G+1).

2) The dominant noise source for the RANS circuit is 1/f noise from the driver transistor. The reasons for this are : (a) Noise from the driver transistor is amplified by the inverter; and (b) 1/f noise is the dominant noise source for MOS transistors in the frequency range of the inverse of tranfer time t (about 1MHz).

Table 1 Noise charge expression ($Crms^2$)

Transfer Gate	Thermal	$\frac{1}{2}kT\frac{C_V}{1+G}$
	1/f	$\frac{q^2 t_{ox}^2 N_{TET}}{\varepsilon_{ox}^2 L_T W_T} U(R_T,t) \frac{C_V^2}{(1+G)^2}$
Load	Thermal	$\frac{4}{3}kT\frac{1}{g_{mL}}\frac{1}{t}\frac{C_V^2}{(1+G)^2}$
	1/f	$\frac{q^2 t_{ox}^2 N_{TEL}}{\varepsilon_{ox}^2 L_L W_L} U(R_L,t) \frac{C_V^2}{(1+G)^2}$
Driver	Thermal	$\frac{4}{3}kT\frac{1}{g_{mD}t}\frac{G^2 C_V^2}{(1+G)^2}$
	1/f	$\frac{q^2 t_{oxD}^2 N_{TED}}{\varepsilon_{ox}^2 L_D W_D} U(R_D,t) \frac{G^2 C_V^2}{(1+G)^2}$

$$U(R,t) = \frac{2^{R-1}\pi^R}{\Gamma(R)\cos(\pi R/2)} \frac{t^{R-1}}{R(R+1)}$$

k: Boltzmann's constant; T: Temperature;
C_V: Capacitance of vertical signal line;
G: Inverter gain; q: Electronic charge;
t_{ox}: Gate oxide thickness; W: Channel length
N_{TE}: Effective trap density; L: Channel width
R: Inclination of 1/f noise spectrum
ε_{ox}: Dielectric constant of SiO_2
t: Transfer time; gm: Mutual conductance

4. MEASUREMENTS

RANS circuit noise currents were measured for different device parameters. It was seen that noise current was reduced proportional to the capacitance of the vertical signal lines, as shown in Fig. 4. Noise also decreased as the channel length of the driver increased, as Fig. 5 makes clear. Device parameters for the transfer gate and load did not affect the noise currents.

These results indicate that the dominant noise source was 1/f noise from the driver. The solid lines in Figs. 4 and 5 express theoretical noise, where noise charges were converted to noise current by

$$I_n^2 = 2F_h F_b q_D^2. \quad \text{----------(8)}$$

Here, F_h is the driving frequency for the BCD, and F_b is the cut-off frequency of the low-pass filter. Mearurements were in good agreement with caluculations, and confirmed our analysis.

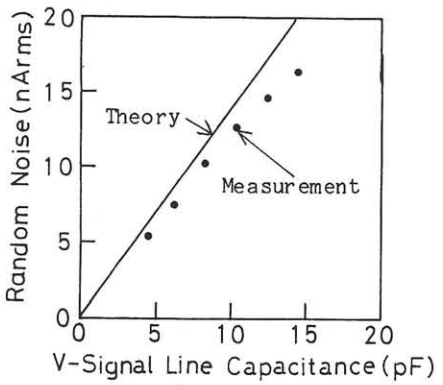

Fig. 4 V-signal line capacitance dependence of random noise in RANS circuits

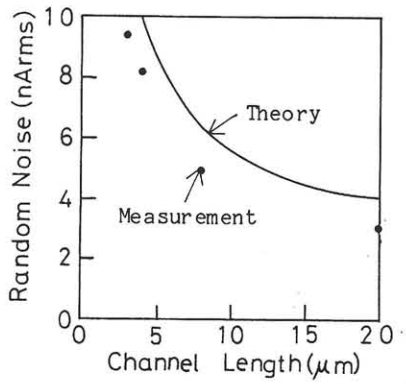

Fig. 5 Driver channel length dependence of random noise in RANS circuits

5. DESIGN COSIDERATION

In order to reduce RANS circuit noise, it is necessary to reduce 1/f noise from the driver. The analytical results shown in Table 1 indicate noise from the 1/f noise of the driver, q_{Df}, can

be reduced by using a long channel length or wide channel width. On the other hand, the total capacitance of the vertical signal line, including the gate capacitance of the driver, is increased as the channel width or channel length is increased. As a result, a minimum random noise value is reached.

q_{Df} can also be expressed in terms of channel dimensions, L_D, W_D, $t_{ox,D}$, by

$$q_{Df}=P\frac{t_{ox,D}}{\varepsilon_{ox}}\frac{C_{VO}+L_DW_D\,ox/t_{ox,D}}{\sqrt{L_DW_D}} \quad ----(9)$$

where P is constant and C_{VO} is the original capacitance of the vertical signal line excluding the gate capacitance of the driver. The minimum value of the noise charge, q_{Dfopt}, can be obtained at $L_DW_D=t_{ox,D}C_{VO}/\varepsilon_{ox}$. That is,

$$q_{Dfopt}=2P\sqrt{\frac{t_{ox,D}C_{VO}}{\varepsilon_{ox}}} \quad ----------(10)$$

The dependence of the noise current on width of the driver is shown in Fig. 6. Noise has a minimum value at $W_D=1000\mu m$.

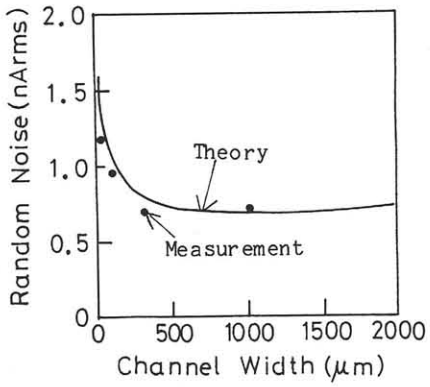

Fig. 6 Driver channel width dependence of random noise in RANS circuits

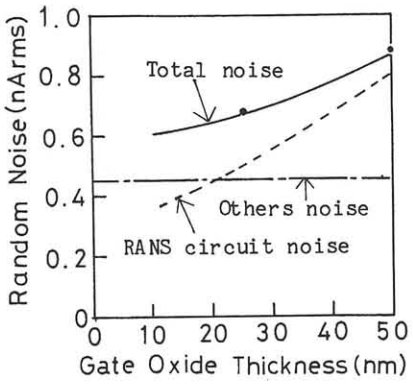

Fig. 7 Gate oxide thickness dependence of random noise in new MOS device

The best way to achieve further improvement is to use thinner gate oxide film. For this case, the total noise current of the new imaging device is reduced as shown in Fig. 7. However, it cannot be improved to the extent indecated by the theory. This is because noise from the vertical switching transistors, BCD, and control gates cannot be considered negligible when compared to noise in RANS circuits.

6. CONCLUSION

A RANS circuits was proposed for suppression of kTC noise. It was found that the dominant noise source in the RANS circuits is 1/f noise at the driver. This noise can be reduced by using a driver transistor with wide channel width as well as thin gate oxide film. As a result, total noise for new imaging device can be made as low as around 0.7nArms with a gate oxide thickness of 25nm, This is only 1/3 of the noise for a conventionl MOS imaging device[2]. Good agreement between experimental results and theoretical values was obtained, based on the noise model, thus indicating the model's validity.

7. ACKNOWLEDGEMENTS

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