Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 511-514

Nucleation Control and Epitaxial Alignment in Silicon-on-Insulator Structure during Solid Phase Growth

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Two possible solutions to the problem of nucleous growth encountered in lateral solid-phase epitaxial growth over insulating films are discussed. Driving force for preferential nucleation in amorphous-Si on SiO_2 films was found to be a stress field originating from the thermal expansion coefficient for Si and SiO_2. Utilization of underlying Si_3N_4 films successfully eliminated such nuclei growth. Additionally, high-temperature annealing ($\geq$ 1000 C) crystallized poly-Si nuclei under lateral epitaxial alignment. Growth speed (v [cm/s]) was estimated to be $1.6 \times 10^6 \exp(-3.9/kT[eV])$.

1. Introduction

Recent developments in lateral solid-phase epitaxy (L-SPE) are raising expectations of establishing a new method of Si-on-insulator (SOI) fabrication. Generation of surface ripple and detrimental crystal defects in the SOI layer, which conventional beam-annealing techniques[1] have encountered, has successfully been overcome. This makes L-SPE very attractive for fabrication of sub-micron and 3-dimensional LSIs.

However, the oriented crystal growth length has been limited to only 5 μm[2,3]. This is because nucleation of the polycrystalline-Si (poly-Si) occurs randomly in the deposited amorphous-Si (a-Si) layer during annealing, which restrains propagation of L-SPE growth. Consequently, techniques that enable (1) enhancement of L-SPE velocity, (2) crystallization of poly-Si nuclei, and/or (3) control of nucleation should be developed to enlarge the L-SPE growth area. Very recently, Yamamoto et al.[4] successfully enhanced L-SPE velocity by doping P^+ ions in the a-Si layer. This extended the L-SPE growth length to 20 μm.

Therefore, we focused our research on developing the other two methods, i.e. (2) and (3). The possibility of single-crystallization from poly-Si into crystal Si was examined first, and epitaxial alignment in the SOI structure was successfully obtained. In addition, nucleation in a-Si layers on insulating films was studied.

2. Experiments

Si substrates ((100) orientation) were covered by SiO_2 stripes and square islands. Thickness of the SiO_2 films were 10 - 100 nm and pattern-edges were made parallel to the [011] axes. After cleaning of the sample surface, Si films were deposited (deposition rate: 0.1 nm/sec, deposition thickness: 1 - 1.5 μm) on the sample surfaces under ultra-high vacuum (UHV) conditions (10^{-10} mbar). During deposition, some samples were kept at 750 C (sample(I)) and others were kept at room temperature (sample(II)). After annealing (400 - 1200 C, 1 - 20 hrs) in a dry N_2 atomosphere, both types of samples were studied by Nomarski optical microscopy and micro-probe reflection high energy electron diffraction (μ-RHEED)[5].

3. Lateral Epitaxial Alignment of Poly-Si

In order to examine the possibility of applying single-crystallization of poly-Si directly deposited on a Si substrate as recently reported by Tsaur et al.[6] and Natsuaki et al.[7] to SOI fabrication, we investigated the annealing characteristics of a molecular-beam-epitaxy sample on a SOI structure, i.e sample (I) described in

section 2 (poly-Si: 1.4 μm thick, SiO_2: 0.5 μm thick). The crystal structure of the as-deposited sample obtained by μ-RHEED is shown in Fig.1-(a). It indicates not only that crystal Si was epitaxially grown on the Si substrate region during deposition ((A)) , i.e molecular beam epitaxial growth, but also that only poly-Si was deposited on the SiO_2 pattern region ((B),(C)). This crystal structure change after annealing was carefully investigated. It was found that structures did not change significantly during low-temperature annealing (< 800 C). However, when the annealing temperature exceeded 1000 C, the poly-Si turned into a crystalline state. Fig.1-(b) shows an example (1150 C, 1 hr) where all poly-Si on the SiO_2 pattern was completely recrystallized. In addition, crystal orientations were exactly identical to that of the Si substrate. This establishes single-crystallization of poly-Si in an SOI structure for the first time. This newly developed method of lateral epitaxial alignment is a useful means of reducing poly-Si nuclei that are randomly generated during L-SPE growth.

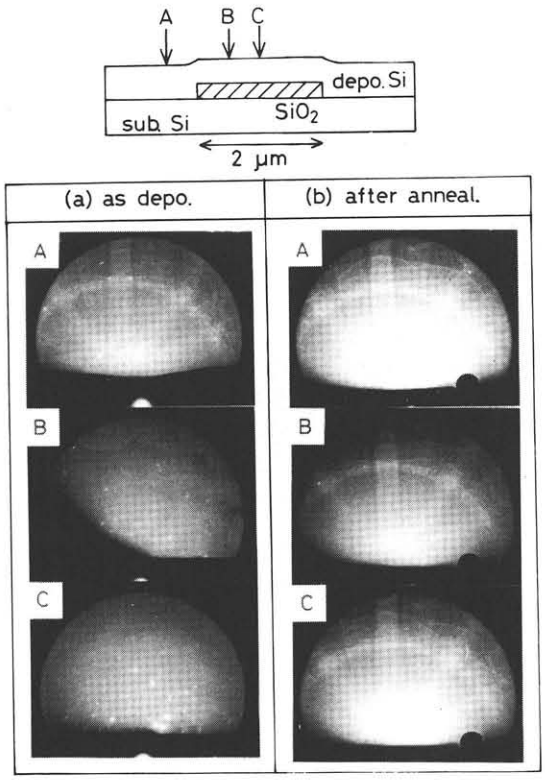

Fig.1 μ-RHEED observation of epitaxial alignment in poly-Si: (a) as-deposited, (b) after annealing (1150 C, 1 hr)

Growth speed under lateral epitaxial alignment was estimated from the various samples. It is compared in Fig.2 with SPE speed[8] (crystallization velocity of a-Si). Alignment velocity (v [cm/sec]) was estimated to be $1.6 \times 10^6 \exp(-3.9/kT[eV])$. This velocity is almost the same as that obtained for vertical epitaxial alignment (single-crystallization of poly-Si on Si)[6,7]. Activation energy of the epitaxial alignment (3.9 eV) corresponds to the self-diffusion energy of Si atoms[9]. This value is twice that of SPE[8]. Consequently, epitaxial alignment is only effective at high temperature annealing (>1000 C). When only low-temperature processing (600 - 800 C) is required for SOI fabrication, control of nucleation in the a-Si becomes more important. This triggered additional research, i.e investigation of the nucleation phenomena.

4. Nucleation Control in Amorphous-Si

Random nucleation in an a-Si layer on SiO_2 film was investigated using sample (II), where

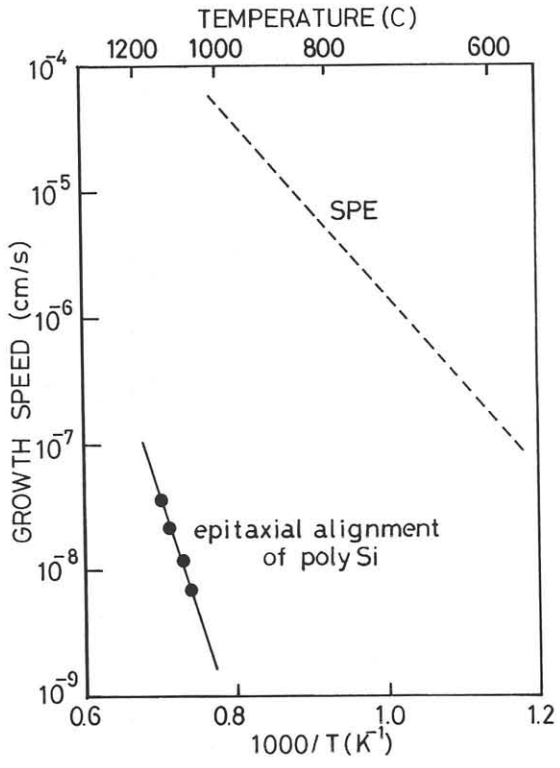

Fig.2 Growth speed of lateral epitaxial alignment in poly-Si and solid phase epitaxy in a-Si

a-Si (1.0 μm) was deposited on SiO_2 films of different thicknesses (0.1 μm and 0.01 μm). One example of nucleation of poly-Si obtained by Nomarsky optical micrograph after furnace annealing (600 C, 3 or 5 hrs) and Wright etching is shown in Fig.3. In that figure, two different types of nuclei are clearly visible. One type is generated ramdomly above the flat SiO_2 region (type(A)). No distinctive phenomena were observed on either thick or thin film regions. The other type of nuclei was found only along the SiO_2 steps (type(B)).

Growth speed of nuclei for types (A) and (B) were measured as a function of annealing temperature. The results are summarized in Fig.4. For type (A) nuclei, activation energy of 2.1 eV was obtained, which corresponds to dissociation energy of the Si - Si bond. However, for type (B) nuclei, activation energy decreased to 1.7 eV. Therefore, only type (B) nuclei were found after the shorter annealing time (Fig.3-(a)). Such nucleation at SiO_2 steps is a serious problem in device fabrication. This is because, in actual device processing, a-Si is deposited on SiO_2 films with complicated structures.

In order to clarify the preferential nucleation mechanism for type (B), crystal orientation of the sample in Fig.3-(a) was examined as a function of depth by a combination of μ-RHEED and etching techniques. The RHEED pattern at the sample surface indicated that the surface region is an amorphous state. A polycrystalline signal was obtained only from the region deep in the deposited Si layer, i.e deeper than 0.5 μm from the sample surface. Stress distribution in Si calculated by Blech et al.[10] and Moniwa et al.[11], which are based on the thermal expansion difference between Si and SiO_2, indicates that a large stress field exists in the Si layer near the SiO_2 films. In particular, they are concentrated at the topographically irregular portions of the SiO_2 films , i.e at SiO_2 steps.

These results suggest that a stress field is the driving force for type (B) nuclei growth. In order to confirm this speculation, nucleation in a-Si deposited on Si_3N_4 films having the same thermal expansion coefficient was investigated. No preferential nucleation at the Si_3N_4 steps was found. This indicates that elimination of stress fields is essential for retarding of nuclei growth.

5. Summary

Annealing characteristics of UHV-deposited Si layers in SOI structures were investigated. Nucleation in a-Si occurred preferentially at SiO_2 steps during low-temperature annealing ($\simeq$ 600 C). Additionally, ellimination of the stress field,

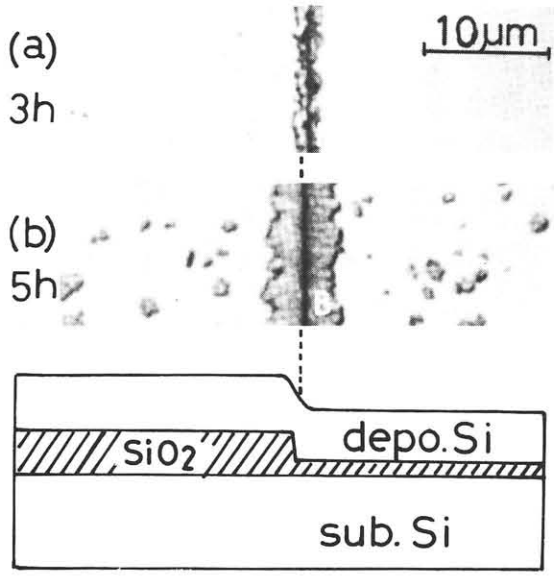

Fig.3 Nucleation of poly-Si in a-Si deposited on SiO_2 films: (a) 600 C, 3 hr annealing, (b) 600°C, 5 hr annealing

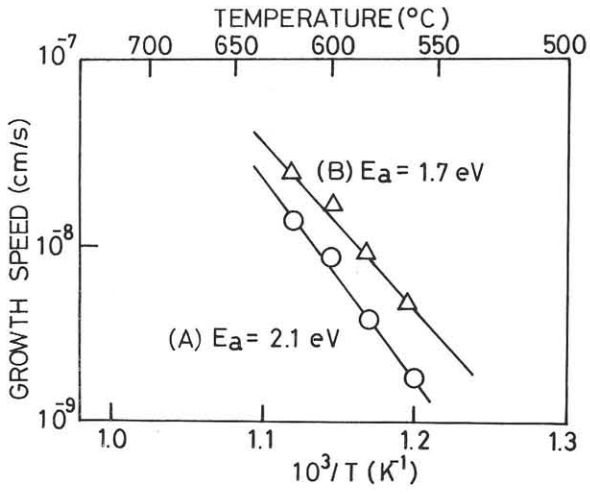

Fig.4 Growth speed of nuclei as a function of annealing temperature: (A) nuclei in the flat SiO_2 region, (B) nuclei at SiO_2 steps

i.e utilization of Si_3N_4 film, successfully retardeed nuclei growth. During high-temperature annealing ($\geq$1000 C), lateral epitaxial alignment of poly-Si was obtained for the first time. This successfully diminished the number of poly-Si nuclei. Both improvements will be of great help in establishing solid-phase-growth SOI.

Acknowledgements

The authors would like to express their thanks to Prof.S.Furukawa, Dr.H.Ishiwara and Mr.H.Yamamoto of the Tokyo Inst. of Tech. for their valuable suggestions and discussions. They also wish to thank Drs. M.Tamura, Y.Shiraki , T.Warabisako and N.Natsuaki of C.R.L Hitachi Ltd. for their helpful comments during the course of this study.

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