

A Completely Planar Type PIN-FETs Using p-Column Gate and High Purity InGaAs Layer for Long Wavelength Region

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New planar type InGaAs/InP PIN-FETs fabricated from the high-purity InGaAs epitaxial layer are proposed. The device employing p-column gate FET provides the same hetero-structure both for the PIN optical absorbing layer and for the FET active layer. p-type regions for PIN and FET are formed by Be ion implantation of single process procedure. The device structure is free from the layer thickness control, which is of great use for developing the OEICs. Static electrical and optical measurement yields a transconductance of about 10 mS and a total effective quantum efficiency of 400 % in the 1.5 μm wavelength region.

1. Introduction

Monolithically integrated optoelectronic devices using GaAlAs or InGaAsP alloy system have been developed so far from the various technical approaches. Among them, PIN-FET employing InGaAs is the most promising for the long wavelength optical receiver, because of its high mobility¹⁾ and band gap matching with the optical fiber transmission spectra. Up to date, InGaAs(P) PIN-FETs have been reported employing pn junction gate^{2,3)} or MIS gate structure⁴⁾, because the Schottky barrier heights on InGaAs are not high enough to be used in MESFET gate⁵⁾.

On the other hand, planar type PIN-FETs have been achieved only by pn junction gate structure employing Zn thermal diffusion. In these devices, the thickness control of the FET active layer is indispensable for adjusting the cut-off voltage. Device structure proposed herein does not need that thickness control for FET active layer, thus the same hetero-structure can be used both for PIN photodiode and for FET area. This merit of thickness-control-free is

of great importance in expanding the OEICs development. The FET employs p-column gate. p-type regions for PIN photodiode and FET are formed by Be ion-implantation. Static optical response exhibits the total quantum efficiency of 400 % in the 1.5 μm wavelength region.

2. PIN-FET Structure and Fabrication

The device structure is shown in Fig. 1. The

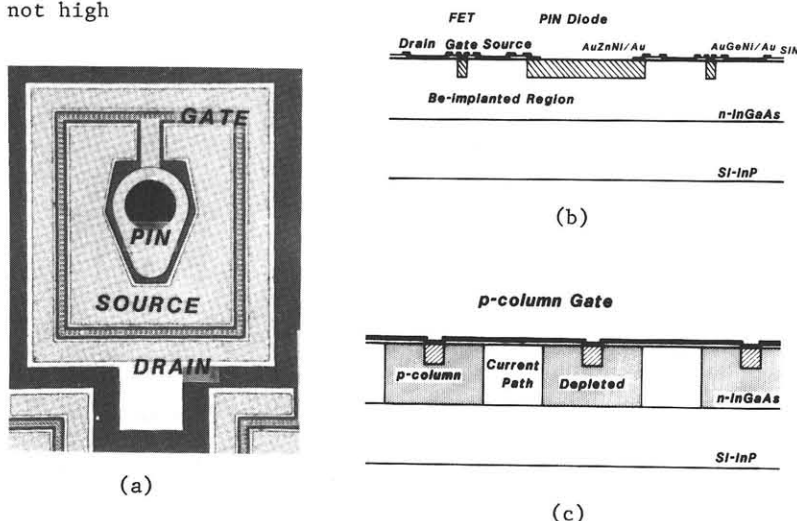


Fig.1 Structure of PIN-FET
 (a) Top view photograph, (b) Cross sectional view across PIN diode and (c) across FET column gate.

PIN photodiode is located in the center of the device and its p-electrode is connected with the FET gate, as shown in Fig. 1(a). The device holds the active layer for PIN photodiode and that for FET in common. Furthermore, the n-source electrode is the common (Fig. 1(b)). The FET employs p-column gate⁶⁾ which controls the electric current by the radial and the axial spread of the depletion layer. The gate bias depletes the InGaAs active layer just under both PIN and p-column of FET. Only several volts of gate bias voltage are required for depleting the high-purity InGaAs layer. The active layer underneath the column can be moreover depleted by the drain bias increase. Therefore, in our devices the cut-off condition can be controlled by adjusting the p-column spacing, as shown in Fig.1(c), thus our device structure is free from the layer thickness control.

The sensitive area diameter of the PIN photodiode is 80 μm and the FET gate geometry consists of about 130 columns of 4 μm square separated by 5 μm each other. The high purity InGaAs layer was grown by liquid phase epitaxy⁷⁾ with carrier concentration of $3.2 \times 10^{14} \text{ cm}^{-3}$, thickness of 2.7 μm , and room temperature mobility of $12,300 \text{ cm}^2/\text{V}\cdot\text{s}$ on (100) oriented semi-insulating InP substrate. Double-energy Be ion implantation of 50 keV with the dosage of $1 \times 10^{14} \text{ cm}^{-2}$ and 200 keV of $5 \times 10^{14} \text{ cm}^{-2}$ has been used to produce simultaneously p-regions both for

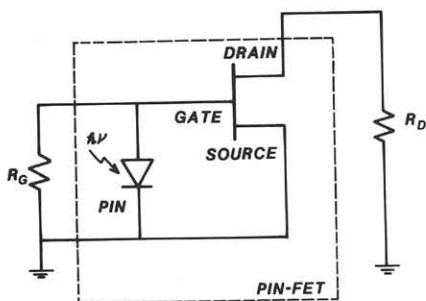


Fig.2 Equivalent (surrounded with dashed line) and operating circuit.

PIN photodiode and for FET gate. The subsequent thermal annealing for 20 minutes at 600°C yielded the resultant p-n junction at approximately 1.3 μm from the surface. During these processes, the implanted InGaAs surface was covered with about 500Å thick silicon nitride film to protect against contamination and to be the encapsulation. Contact was made to the Be-implanted region using AuZnNi/Au, while AuGeNi/Au was used to the common and drain n-type electrode.

3. Static Electrical Characteristics

The operating circuit in common-source configuration for the PIN-FET is shown in Fig. 2. Monolithically integrated PIN-FET is indicated here within dashed line. R_G and R_D are the external load resistance to a PIN photodiode and an FET, respectively. R_G also plays a role as a gate load resistance for applying the input signal to an FET.

In Fig. 3(a), the measured source-to-drain current variations with the gate voltage are shown. These static characteristics show current cut-off at the gate bias of -4 volt and

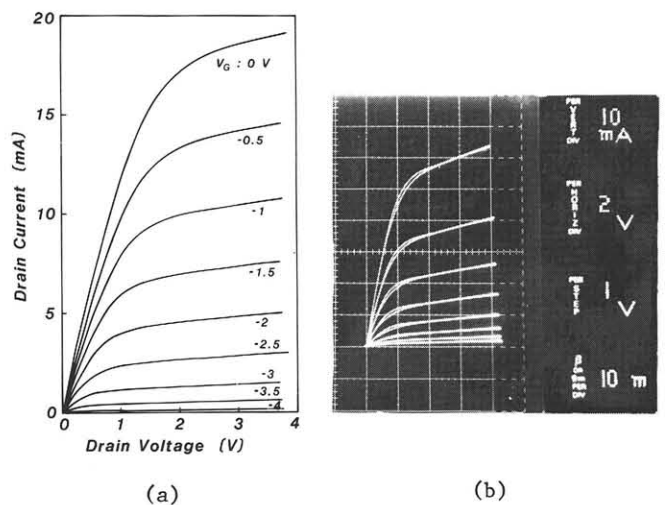


Fig.3 Static drain-source current variation vs. drain voltage of device fabricated from InGaAs layer with carrier concentration of (a) less than $1 \times 10^{15} \text{ cm}^{-3}$ and (b) more than $1 \times 10^{16} \text{ cm}^{-3}$.

saturation current of about 20 mA. Analysis of these static characteristics gives a transconductance $G_m \approx 10$ mS around zero gate voltage. In order to take advantage of the integrated PIN-FET optical receiver, high transconductance and low capacitance (C_T) are required. We have obtained a transconductance of about 20 mS by using InGaAs epitaxial layer with higher carrier concentration of $1.2 \times 10^{16} \text{ cm}^{-3}$ (Fig.3(b)). In this device, PIN photodiode has almost the same photoresponse characteristics as that of the device fabricated from the high purity InGaAs layer.

The gate leakage current, which includes the photodiode dark current, under the reverse bias condition with drain open circuited was measured to be about 50 nA at -5 volt. The gate leakage current contributes to the receiver noise, particularly being dominant for low bit-rate applications of less than 10 Mbit/s⁸).

4. Static Optical Characteristics

Figure 4 shows the gate-to-source voltage (V_D) dependences of the static photocurrent gain in common-source configuration under the condition that drain-to-source voltage (V_D) is 5

V, $R_D=R_G=1$ kohm, and wavelength 1.55 μm . In this figure, gate-source characteristics, indicated by solid circles, correspond to the photodiode output exhibiting the saturation under reverse bias condition and yielding quantum efficiency of about 70 %. On the contrary, drain-source one by open circles showing the FET output decreases with increasing gate bias toward the cut-off condition of about -4.5 V. Static photocurrent gain characteristic against gate load resistance in common-source configuration at 1.55 μm wavelength is also shown in Fig.5. Drain-source characteristic by open circles is obtained with R_D of 1 kohm in common-source configuration, which is well analogous to the gate-source one. From these characteristics the current gain of about 5.8 can be derived when $R_G=R_D=1$ kohm and such bias conditions as $V_G=-0.6$ V, $V_D=5$ V, respectively. The results shown in Fig.4 and 5 coincide well with calculation using G_m measured electrically from Fig. 3(a). The total effective quantum efficiency can be estimated to be about 400 %.

We show the photocurrent gain characteristic as a function of input optical power in Fig. 6. It is shown that our PIN-FET exhibits good linearity against input optical power up to several hundreds of micro watt.

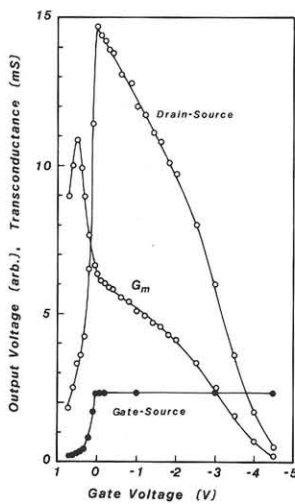


Fig.4 Static optical response vs. gate-to-source voltage.

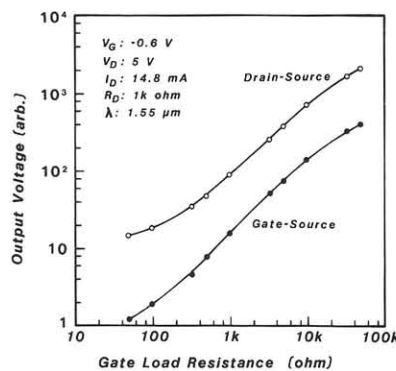


Fig.5 Static photocurrent gain characteristics vs. gate load resistance.

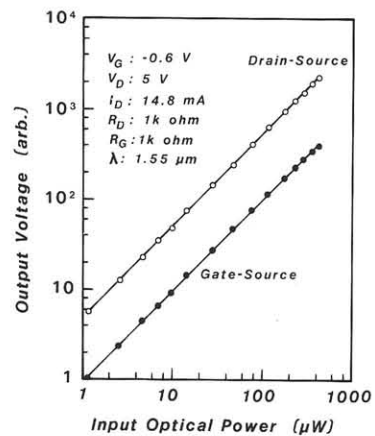


Fig.6 Static photocurrent gain vs. input optical power.

5. Summary

The planar InGaAs/InP PIN-FETs have been fabricated from the high purity InGaAs epitaxial layer, which hold the same active layer for PIN photodiode and that for FET in common. p-type regions of PIN photodiode and FET gate column were formed employing the double-energy Be ion implantation. The advantage of the freedom from active layer thickness control should be of great importance for developing the OEICs. Static electrical and optical measurement yields a transconductance of 10 mS, a photocurrent gain of 5.8 in common-source configuration and a total effective quantum efficiency of 400 %.

6. Acknowledgement

The authors are deeply indebted to K.Kurumada for his valuable discussions and suggestions. They would like to thank H.Nagai and K.Asai for helpful discussions and T.Honda for cooperation in ion implantation, and they would also like to acknowledge encouragements by M.Fujimoto and T.Ikegami throughout this work.

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