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Monolithic Integration of InGaAsP/InP Laser Diode with Heterojunction Bipolar Transistors

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We report the first successful integration of a laser diode of 1.3μm wavelength range and high speed driving circuits. In the optoelectronic integrated circuit, a buried heterostructure laser diode and three heterojunction bipolar transistors are fabricated by using InGaAsP and InP Liquid Phase Epitaxial layers grown on a single InP substrate. Due to the high emitter efficiency resulting from the heterostructure, heterojunction bipolar transistors with high speed performance have been achieved. As the results, this new optoelectronic integrated circuit has been confirmed to be operated at the frequency up to 1.6GHz and the modulated laser output was observed.

§1. Introduction

Optical fiber communication systems, which have a potential capability of transmitting a huge quantity of information compared with the conventional electric systems, will be the main communication media in the coming highly intelligent information society. And practically, the optical fiber communication systems have been being steadily developed with the development of the optoelectronic devices, especially at 0.8μm and 1.3μm wavelength range. In these systems, the optoelectronic devices such as laser diode (LD) and photo-detector (PD) are driven or controlled by external electrical circuits. However, the limited operation speed due to their lead and wire inductances and the stray capacities is the serious problem for the high speed fiber optic transmission. Therefore, the integration of optoelectronic devices and electronic circuits on the same substrate is considered to be a key technology. This will give not only high speed performance, but multifunction and reliability. In this respect, the integration of optoelectronic and electronic devices based on InP or GaAs compound semiconductors substrate, e.g. LD/field effect transistor (FET)[1-4], light emitting diode (LED)/FET[5], PIN/FET[6] and LD·PD/FET[7] etc., were reported.

We have integrated a LD of 1.3μm wavelength range and its driving circuits by using InGaAsP/InP semiconductor layers. The LD has a buried heterostructure and Fabry-Pérot resonators, and we adopted heterojunction bipolar transistors (HBT's)[8] for LD driver because of the high speed performance and the compatible with the LD fabrication process. In order to attain the same operation voltage level as emitter coupled logic (ECL) IC's, the driving circuits which consist of a differential type circuits comprising three bipolar transistors were employed. This report describes the fabrication process and the performance of the new LD/HBT's OEIC.

§2. The Design of the OEIC

The cross sectional view of the fabricated OEIC is schematically shown in Fig.1. The laser diode has a typical BH laser diode structure except the point that the buring epitaxial layers consist of four layers, which are also utilized for the HBT's fabrication. Equivalent circuit diagram of the OEIC in this study is shown in Fig. 2. Differential type circuit comprising three HBT's is fabricated for high speed modulation of the laser diode. The supply voltage (V^-) was designed to be -5.2V in order to be compatible with ECL IC's.

The HBT, which is able to make use of buring epitaxial layers, is considered to be suitable for the planar structure. We compared a junction field effect transistor (J-FET) and a bipolar

transistor as the active drive element of LD on InP epitaxial layer. By assuming the carrier concentration of buring epitaxial layer to be $1x10^{16}$ cm^{-3} and the maximum current to be 60mA, we calculated cell size, channel conductance, pinch off voltage and common emitter current gain for both J-FET and bipolar transistor. For the J-FET, when the ratio of the gate width to the gate length (Wg/Lg) is 60, the channel thickness is 1μm, the number of gate is 2 and the finger length is 150 μm, the cell size, the channel conductance and the pinch off voltage are calculated to be 170μmx95μm, 28.8ms and 6V, respectively. For the bipolar transistor, when we design the emitter-base junction area to be 20μmx20μm, the base width to be 0.2μm, the carrier concentration of base layer to be $1x10^{17}cm^{-3}$, the diffusivity of electron to be $90cm^2$/sec and the contact area of emitter, base and collector to be 10μmx10μm, 5μmx15μm and 5μmx20 μm, respectively, the cell size and common emitter current gain of the bipolar transistor correspond to 70μmx50μm and 200, respectively. Generally, current-voltage characteristics of the J-FET and the bipolar transistor are expressed by the following equations as $I_{DSS} \propto (V_p - V_{GS})^2$, $I_C \propto \exp(qV_{BE}/nkT)$, respectively. Where, I_{DSS}: the drain current in the saturation region, V_p: the pinch off voltage, V_{GS}: the voltage at the gate-source junction, I_C: the collector current, q: magnitude of electronic charge, V_{BE}: the voltage at the base-emitter junction, n: the ideal factor at the base-emitter junction, k: Boltzmann's constant, T: the temperature. Therefore, the input voltage necessary for the current switching in the differential type circuits using the J-FET and the bipolar transistor are considered to be about $2V_p$=12V and 4kT/q=100mV, respectively. Due to low input voltage property of the bipolar transistor, high speed operation of LD driving circuits will be possible.

Then the suitable structure of the bipolar transistor for the fabrication is considered based on the device fabrication process such as the liquid phase epitaxial growth and the zinc diffusion process. The carrier concentration of the collector layer (n-InP) and the emitter layer (n-InP) should be lower than that of Zn at the surface, because of the graft base structure, giving low base resistance and the isolation area, are formed in these layers by the thermal diffusion of the zinc.[9] Under the restrictions described above, we concluded that the heterojunction bipolar transistor (HBT) is the most suitable for a high emitter efficiency. Due to

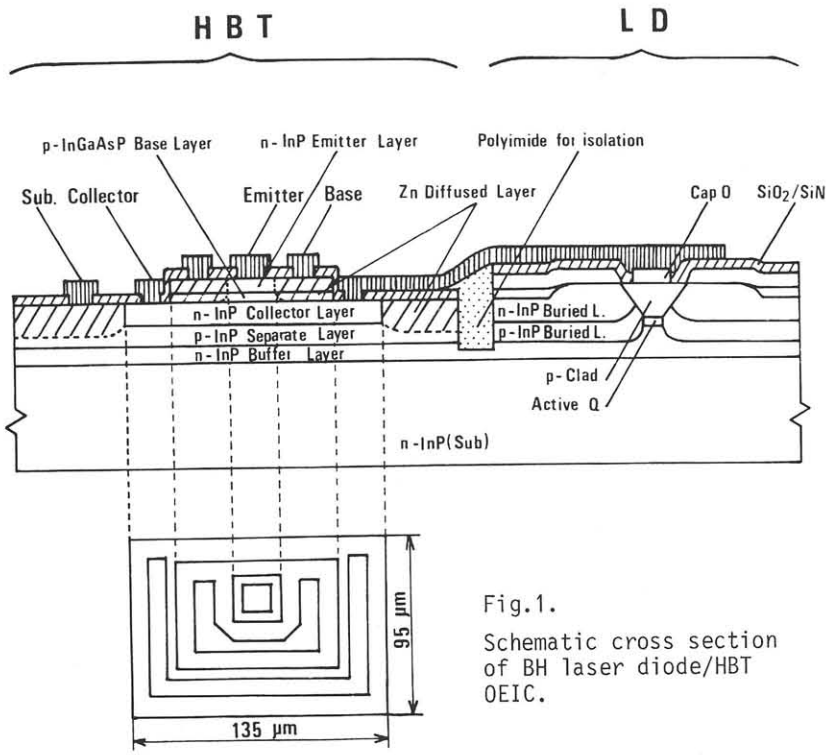

Fig.1.
Schematic cross section of BH laser diode/HBT OEIC.

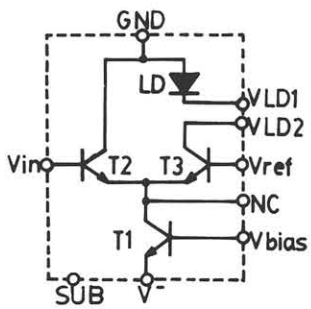

Fig.2.
Equivalent circuit diagram of the fabricated OEIC.

the heterostructure, a high common emitter current gain and a high speed performance was obtained even though carrier concentration of the emitter layer was lower than one of the base layer.

§3. Fabrication Processing of the OEIC

The fabrication process of the OEIC is as follows. The BH laser diode was fabricated in conventional manners as follows. At first, p-InGaAsP(Cap)/p-InP(p-clad)/InGaAsP(active Q, λg=1.3μm)/n-InP(n-clad, buffer) layers, which is constructing a double heterostructure, was grown on (100)-oriented n^+-InP substrate by liquid phase epitaxy (LPE), and then etched through SiO_2 mask, which is fabricated on the layers, by $HCl:H_3PO_4$ (1:2) and Br_2-methanol to make the laser stripe. The laser stripe was then buried with the four LPE layers: p-InP (1.5μm thick, $1x10^{17}cm^{-3}$), n-InP (2.5μm thick, $1x10^{17}cm^{-3}$), p-InGaAsP (0.2μm thick, $1x10^{17}cm^{-3}$, λg=1.1μm), n-InP (0.7μm thick, $5x10^{17}$ cm^{-3}), which would also be the separate layer, collector layer, base layer and emitter layer of the HBT's, respectively. The impurities doped into the layers were Te and Zn for n and p layers, respectively. Emitter layer (n-InP) and base layer (p-InGaAsP) were selectively etched by photolithographic technique using $HCl:H_3PO_4$ (1:2) and $H_2SO_4:H_2O_2:H_2O$ (1:1:5), respectively. The p regions were formed by Zn diffusion. The diffusion was carried out at be 500°C in order to give a sufficient Zn concentration as well as to avoid the thermal damages and auto-doping effects between each layer. The diffusion time for the isolation of each HBT was 70 min. and that for the graft base structure was 15 min. In order to isolate the laser diode from HBT's electrically, a groove was formed on the surface layer by etching to the n-InP buffer layer and then the groove was buried with polyimide to give a smooth surface metallization between the laser diode and the HBT's. Au/Zn/Au was deposited and patterned by lift off technique to give an ohmic contact on the base, isolation region and p-side of the laser diode, and Au/Sn/Au was deposited on collector and emitter as well as n-side of the laser diode. Final metallization for the interconnection between each element was done by the deposition of Ti/Au on SiN/SiO_2, then alloyed at 420°C for 5 min. to give an ohmic contact. Figure 3 shows the photograph of the OEIC's, which is taken before the cleavage to make Fabry-Pérot mirrors. The chip size is 350μmx910μm.

§4. Characteristics of the fabricated OEIC and Discussions

The threshold current of the laser diode of the fabricated OEIC was 20∿30mA at room temperature, and both single transverse and longitudinal mode oscillation was observed up to the output light power of 10mW. The external quantum efficiency of the laser diode was measured to be 20%. The laser characteristics were similar to that of the discrete laser diodes except the point that the threshold current was a little bit larger because of the poor heat dissipation owing to the n-side down mounting. Figure 4 shows the current-voltage characteristics of a single HBT of the fabricated OEIC. The typical common emitter

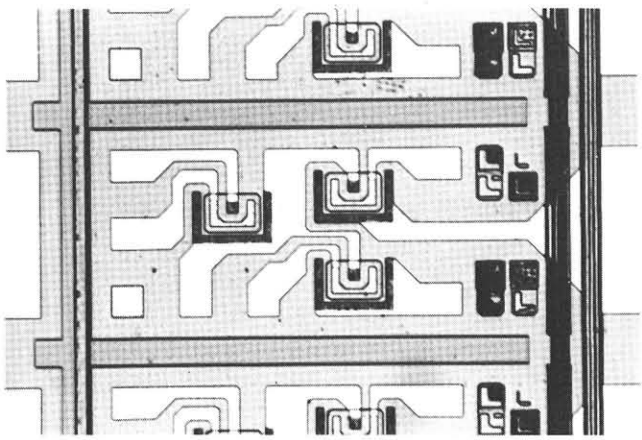

Fig.3. A photograph of the fabricated OEIC's, which is taken before the cleavage to make Fabry-Pérot mirrors. The chip size is 350μmx910μm.

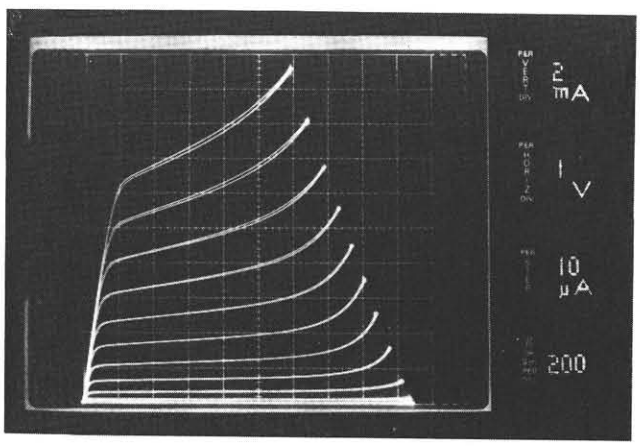

Fig.4. Typical current-voltage characteristics of a single heterojunction bipolar transistor.

current gain (h_{FE}) was about 400 at the collector current of 60mA. At this collector current, transition frequency of HBT evaluated by S-parameter measurements was about 1.1GHz. Breakdown voltage between the collector and the base, which is giving the collector current of 10μA, was about 20V. Figure 5 shows the optical response properties of the developed OEIC, which is measured by a photodetector (PIN/FET)[10] with 200psec response time. By applying sinusoidal voltage (0.8V peak to peak) between V_{in} and V_{ref} with dc bias current of 35mA, supplied from external circuit, high frequency modulation up to 1.6GHz for the laser output was achieved.

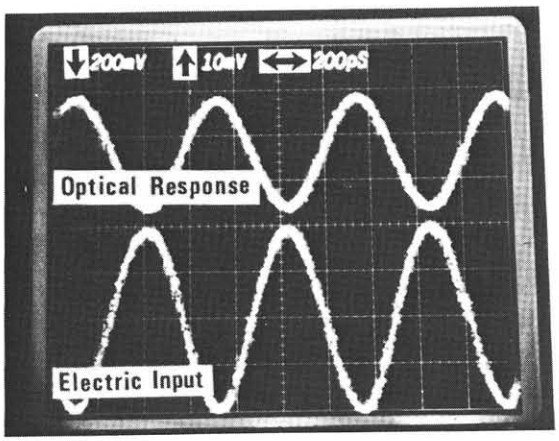

Fig.5. Optical response characteristics: the sinusoidal electrical signal is input between V_{in} and V_{ref} with dc bias current of 35mA. The horizontal scale is 200psec/div.

§5. Conclusion

In summary, we have successfully fabricated the OEIC, which comprise 1.3μm BH laser diode and three heterojunction bipolar transistors (HBT's), based on InGaAsP/InP epitaxial layers on InP substrate. A high common emitter current gain (h_{FE}) of the HBT enables the OEIC to be operated in high speed and 1.6GHz modulation of the laser output was achieved.

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