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Recent Advances in GaAs/(Ga, Al) As Heterojunction Bipolar Transistors

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A review of the potential benefits, technology status, and current performance of GaAs/(Ga,Al)As HBTs is provided, with particular emphasis on recent results obtained at Rockwell International. Graded composition base regions, ion-implanted structures fabricated using rapid thermal annealing, and buried oxygen-implanted isolation regions are highlighted. Ring-oscillators with 29.3 pS propagation delays per gate and frequency dividers operating to 8.5 GHz are reported.

I. HISTORICAL PERSPECTIVE

The desirability of wide bandgap emitters to enhance bipolar transistor performance was noted by Shockley before 1950, and elaborated in independent work by Kroemer in 1957 [1]. Attempts to realize HBT structures were not fruitful until the development of the GaAs/(Ga,Al)As system [2,3]. LPE was initially used to demonstrate high dc performance potential. The development of MBE and MOCVD has more recently brought the promise of attaining highly complex, ultrafast transistor structures with IC-compatible uniformity and large substrate size [4-8]. Average electron velocity above the saturation velocity have been demonstrated and cutoff frequency f_t above 25 GHz has been obtained [6,8]. This research coincides with a period when fundamental material limitations are perceived to adversely affect the rapid performance advancement of Si devices.

II. MOTIVATION FOR HBTs

Table IA lists a number of advantages and disadvantages of GaAs/(Ga,Al)As HBTs in comparison with Si bipolar transistors. Table IB provides a similar comparison between HBTs and GaAs or heterostructure FETs. The considerable benefits of the HBT structure suggest that this will be a preferred approach in the domain of high-speed devices (at least up to moderate integration levels). Cutoff frequencies have been predicted to be as high as 100-150 GHz [9,10].

Table I A - Comparison of GaAs/(Ga,Al)As and Si for Bipolar Transistor Implementation

Relative Advantage of GaAs/(Ga,Al)As
• Variable bandgap allows implementing wide gap emitter, wide gap collector, graded base, etc.
• High electron mobility.
• Electron transient velocity overshoot possible.
• Semi-insulating substrate.
• No problems with surface inversion or accumulation.
• Very high current density feasible.
• Compatibility with optoelectronics.
• Low n_i; isolation through deep levels possible.
• Radiation hardness.
Relative Advantage of Si
• Stable oxide with low surface state densities for isolation.
• Very flexible doping technologies.
• Low surface recombination velocity.
• Withstands high temperature processing.
• Low deep level densities.
• Ohmic contacts obtained easily.

Table IB - Comparison of Bipolar and FET Structures for High Speed Digital Circuits

Relative Advantage of Bipolar
• High transconductance
• High f_t with modest lithography
• High uniformity of threshold voltage
• Low sensitivity of propagation delay to fanout
• Low impedance, high current output drivers easily implemented
• Current steering logic easily implemented
• Insensitive to surface effects or backgating
Relative Advantage of FET
• High input impedance
• Does not store charge in saturation
• Threshold voltage adjustable to any desired value
• Less demanding of ohmic contact quality.

III. HBT TECHNOLOGY ASPECTS

Appreciable technology development remains to be done to realize the high performance predicted for HBTs, since the device processing is significantly different from that of Si bipolars as well as that of GaAs FETs. This paper focuses on technology pursued at Rockwell International, which to date has been based on quasi-planar, ion-implanted, emitter-up, single heterostructure, MBE-grown HBTs oriented towards digital integrated circuits of the ECL family.

The vertical structure of the devices is described in Table II. The doping of the emitter is selected to minimize emitter capacitance, yet provide the necessary current densities without ohmic drops or current saturation. The aluminum fraction is chosen so that the hole injection is minimal ($x \sim 0.25$ to 0.30). An abrupt emitter-base interface gives rise to a "spike" in the conduction band energy profile, as pictured in Fig. 1. This spike decreases collector current and emitter injection efficiency, but can provide injection of high velocity electrons into the base to reduce transit time. To increase the current gain, the conduction band spike may be eliminated by grading the aluminum concentration over a distance of 200-300Å or more. In this case the entire difference in bandgap between the emitter and base contributes to increasing the barrier for hole flow from the base to the emitter, ensuring a high value of emitter injection efficiency.

Table II - Typical Epitaxial Structure for HBTs

Layer	Thickness (μm)	Type	Doping (cm^{-3})	AlAs Fraction	
8	0.075	n^+	$1x10^{19}$	0	Cap
7	0.125	n	$5x10^{17}$	0	Cap
6	0.03	n	$5x10^{17}$	.30-0	Grading
5	0.22	n	$5x10^{17}$	.30	Emitter
4	0.03	n	$5x10^{17}$	0-.30	Grading
3	0.1	p^+	$5x10^{18}$	0	Base
2	0.5	n^-	$3x10^{16}$	0	Collector
1	0.6	n^+	$4x10^{18}$	0	Subcollector
Substrate		S.I.	undoped	0	

A recent innovation is to include a slight amount of Al in the base, grading its concentration from a high value (5-10%) near the emitter to a low value near the collector (0%). The resultant grading of bandgap gives rise to a quasi-electric field that drives electrons across the base. Quasi-electric fields of the order of 5-10 KV/cm may be easily produced, so that electron velocities above 10^7 cm/s may be maintained.

The lateral structure of the transistor is depicted in Fig. 2. Optical contact lithography has been used to date, to achieve emitter widths in the range 1-2 μm.

One of the critical steps in device fabrication is the annealing of the p-type extrinsic base implants. High electrical activation of the implant tends to require high-temperature annealing. On the other hand, it is vital to minimize diffusion of the implanted species and of the epitaxially grown-in doping profiles. In particular, if the Be grown into the base diffuses significantly into the emitter (Ga,Al)As, the emitter-base junction can become a homojunction in the wider bandgap material, with very poor emitter injection efficiency and reduced transistor current gain. Effects of Be diffusion are evident in high turn-on voltage for collector current flow as a result of high temperature annealing. An appropriate solution has been found in the recently introduced rapid thermal annealing processes, in which implants are activated in heating cycles of 10-15 s duration - too short for significant dopant diffusion.

Extrinsic base-collector capacitance (originating from the junction of the p^+ base implant and the collector epilayer) can have a significnt effect in slowing the device performance. To overcome this problem in Si bipolar devices the Sidewall Contact Structure, with SiO_2 spacer layers, has been introduced [11]. Kroemer has pointed out that an inverted transistor structure (with collector on the wafer surface) can also alleviate the problem in the realm of HBTs [1]. Recent work at Rockwell has illustrated an additional simple solution. Oxygen ions (in sheet concentrations of the order of 10^{14} cm^{-2}) are introduced by implantation from the surface into the low doped collector region below the extrinsic base. Oxygen implanted GaAs remains compensated even after high temperature anneal [12]. Semi-insulating spacer layers are therefore formed at the B-C junction which, if sufficiently wide, decrease the B-C capacitance dramatically.

IV. CURRENT HBT PERFORMANCE

The dc characteristics of a representative HBT for use in digital integrated circuits are shown in Fig. 3. The emitter dimensions for the device are 1.6 μm × 5 μm. The device can carry up to 8 mA of collector current (exceeding the current-carrying capability of Si bipolar transistors of comparable size). The transconductance of the device reaches the value of 6000 ms/mm, considerably greater than for any field-effect transistor. Incremental current gain of the transistor reaches 30-40. This is enough for high-speed digital logic applications (for which a current gain of 20-25 may be regarded as the minimum).

A high degree of uniformity of device characteristics, particularly threshold voltage, is required for integrated circuits. Such uniformity is expected to be much better for bipolar transistors than for field effect transistors. Experimental results readily confirm this. Figure 4 shows measured values of output current vs input voltage for a sequence of 15 test transistors located at 2 mm separations across an HBT wafer (16 × 19 cm^2). Defining threshold voltage as the base-emitter voltage required to obtain 0.1 mA of collector current, a standard deviation of threshold voltage of 3.8 mV was computed. Even this low value may be improved upon by superior lithography (such as projection lithography) or by use of larger transistor dimensions; the threshold voltage standard deviation for larger devices (with 8 μm × 20 μm emitters) was 0.8 mV.

The prototype digital circuits used to demonstrate the capabilities of HBT technology include ring oscillators and frequency dividers. The ring oscillators are of the nonthreshold-logic (NTL) type, as well as of the current-mode logic (CML) and classical emitter-coupled logic (ECL) types. The NTL gates, while not adapted to use in complex digital systems because of limited fan-out, are the simplest, and the ones whose characteristics are most directly tied to the transistor charateristics. NTL ring-oscillators with 17 stages were made and propagation delay times per gate of 29.3 ps (at a power of 4 mW per gate) were measured. Relatively low power operation was also observed (60 ps at 400 μW, for a power-delay product of about 25 fJ). A completed NTL ring oscillator is shown in Fig. 5; the speed-power tradeoff for several structures is illustrated in Fig. 6.

Frequency dividers were configured from master/slave D flip-flops implemented with series-gated CML circuits. These classical Si-like circuits allow operation with a single-ended clock at frequencies up to 1/2 τ_d where τ_d is the propagation delay per (complex) gate. Divide by four circuits of this type have been demonstrated which operate at input clock rates up to 8.6 GHz.

Results obtained with the frequency dividers provides a preliminary indication of circuit yield, which appears to be excellent. The yield of: 24 circuits was 90% on the wafer tested. Moreover, this yield result corresponds to rf functionality (with a test frequency input of 7 GHz) using fixed power supply voltages. The dividers are small-scale circuits with 35 transistors in about 15 equivalent gates.

For both ring oscillators and frequency dividers, the circuit operation was found to be in good accord with SPICE simulations based on calculated and measured characteristics of the transistors. Such agreement tends to simplify the task of circuit design. Parameters corresponding to a representative transistor for use in integrated circuits are shown in Table III.

Table III - HBT Model Parameters (SPICE)

Emitter Dimensions	1.6 μm × 5 μm
R_E	28 Ω
R_B	390 Ω
R_C	65 Ω
τ_F	2.5 pS
C_{jeo}	11 fF
C_{jco}	17 fF

V. FUTURE OUTLOOK

A variety of improvements in HBT technology may be anticipated in the future. These include size reduction and improved dimensional control through the use of projection lithography and electron beam lithography, reduction of parasitic resistances and capacitances through the introduction of self-aligned fabrication techniques; and improved current gain and cutoff-frequency through improved undertanding and optimization of the device structure. The use of new material systems may provide additional performance benefits.

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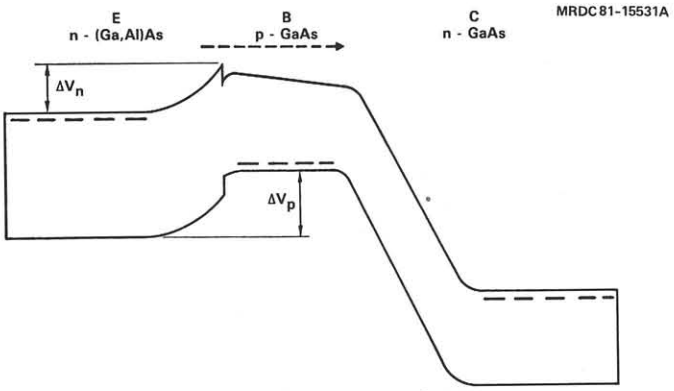

Fig. 1 Schematic band diagram of HBT.

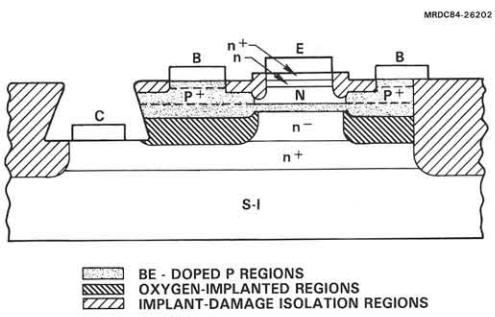

Fig. 2 Schematic cross-section of HBTs fabricated at Rockwell.

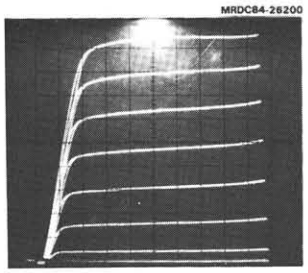

Fig. 3 I_C-V_{CE} characteristics of typical HBT for digital circuits.

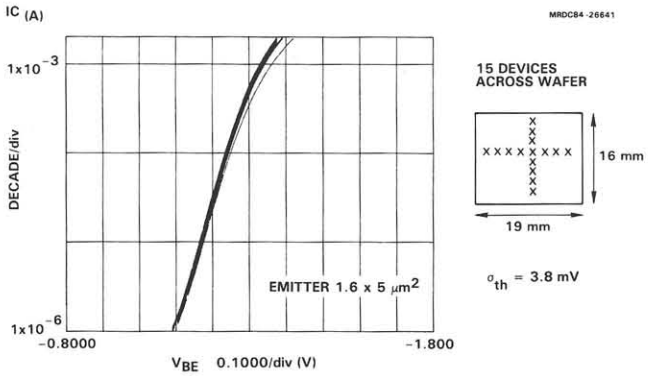

Fig. 4 I_C-V_{BE} characteristics measured on a series of 15 HBTs distributed across a wafer.

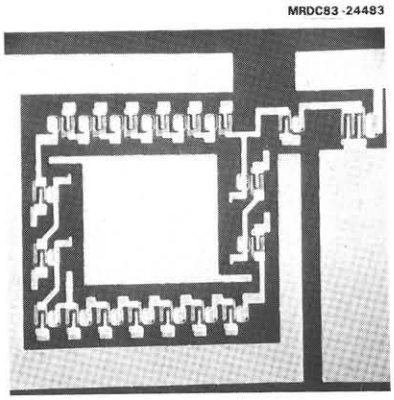

Fig. 5 Photomicrograph of NTL ring-oscillator.

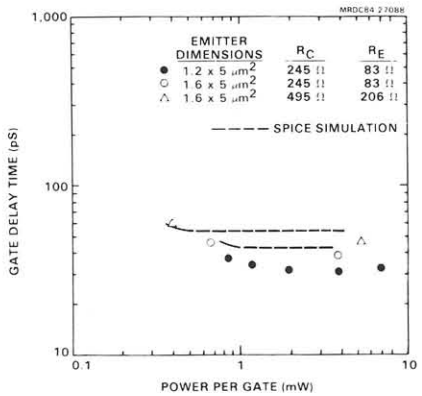

Fig. 6 Speed-power tradeoff measured experimentally and simulated by SPICE for NTL ring-oscillators.