Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 347-350

Low Noise HEMT with Self-Aligned Gate Structure

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Low noise HEMTs (High Electron Mobility Transistors) with self-aligned gate structure have been successfully developed using direct electron beam lithography and selective-dry etching technique. Their source resistances are reduced to one half of the previous result. The 0.4 μm gate length HEMT yielded 1.08 dB noise figure with 12.7 dB associated gain at 12 GHz and 1.7 dB noise figure with 8.8 dB associated gain at 20 GHz. These are comparable to the best results yet reported for quarter-micron gate GaAs MESFETs.

1. Introduction

HEMT based on a selectively doped GaAs/n-AlGaAs single heterojunction structure offers new possibilities for microwave devices [1], [2], [3]. Higher frequency operation and lower-noise performance than GaAs MESFETs are expected of HEMTs, due to high electron mobility and high saturation velocity of a two-dimensional electron gas (2DEG) at the heterojunction interface.

We have already reported on the microwave performance of HEMT with 0.5 μm gate length[1]. Its cut-off frequency is 30 GHz which is 20 % higher than GaAs MESFETs and its noise figure is 1.4 dB at 12 GHz.

To make further improvement in noise performance, it is necessary to know the relation between noise figure and device parameters of HEMT. For GaAs MESFETs, there is the well-known formula obtained by Fukui[4]. For HEMT, recently, Wu et al.[5], calculated the drain thermal noise and gate induced noise, using the simple drain current model. However their calculation did not include the parasitic resistance effect. In an actual device, parasitic resistances play an important role in determining a device noise figure. Thus, in addition to their calculation model, we take account of parasitic resistance effect. We followed their calculation to obtain insight into the HEMT noise performance relative to device parameters.

The calculation result shows that HEMT with shorter gate length and with lower source resistance has the lower noise figure. To reduce source resistance we developed the self-aligned gate technique. It uses an anisotropic dry etching technique instead of wet-chemical etching. The device with self-aligned gate structure exhibited the extremely low noise figure of 1.08 dB at 12 GHz.

This paper describes the noise figure calculation, fabrication process and noise performance of self-aligned gate HEMTs.

2. Modeling of HEMT noise figure

In the calculation of HEMT noise figure, it is assumed that electron mobility is constant throughout the channel, and that drain current saturation occurs when the electric field in the channel reaches the critical value E_c. The drain current in a HEMT device is determined by

$$I_d = \mu (C_g/L_g)(V_g - V_{off} - V(x))(dV/dx) \quad ,$$

where μ is the mobility, $C_g = \varepsilon W L_g/d$ is the gate capacitance, W is the channel width, L_g is the gate length, d is the AlGaAs thickness, ε is the dielectric constant of AlGaAs, and V(x) is the channel potential at x. The only noise considered in this model is the Johnson noise. The noise at the drain current saturation region is not

considered, since the noise figure does not change significantly with increasing drain voltage once the knee point of drain current has been reached. The HEMT noise figure is calculated at the knee of the drain current-voltage characteristics. Also we ignored the hot electron effect. To calculate the noise figure, we used the expression of the power spectrum density of drain thermal noise and induced gate noise which are calculated by Wu, et al.,

$$S_{I_d} = 4kTg_mP \ , \qquad S_{I_g} = 4kT\omega^2C_g^2P/g_m$$

We also used the expression for the minimum noise figure of a GaAs MESFET obtained by Pucel, et al. [6],

$$F_{min} = 1 + 2(\omega C_g/g_m)\sqrt{K_g(K_r + g_m(R_s + R_g)} \qquad (1)$$

$$K_g = P[(1-C\sqrt{R/P})^2 + (1-C^2)R/P]$$

$$K_r = PR(1-C^2)/K_g \ ,$$

where P is drain noise coefficient, R is gate noise coefficient, C is noise correlation coefficient, R_s is a source resistance and R_g is a gate resistance.

When parasitic resistances remain, the second term of the square root in Eq. (1) makes the main contribution. To first order approximation, when the Kr term is ignored, the optimum value F_o of the minimum noise figure can be described by,

$$F_o = 1 + 18\, f\, L_g\sqrt{\varepsilon W(R_s + R_g)/(d\,\mu\, E_c)} \qquad (2)$$

where f is operating frequency. Eq. (2) shows that a device with a thicker AlGaAs layer and with a smaller gate width has a lower optimum noise figure. As a result, small C_g devices and low g_m devices are expected to have a low noise figure. Since gate fringing capacitance is not considered in this model, there should be an optimal value for AlGaAs thickness and gate width.

Fig. 1 shows the dependence of the optimal value of the minimum noise figure on the gate length and the parasitic resistances. It can be seen, like the result obtained by semi-empirical formula [4], that shortening the gate length and minimizing the parasitic gate and source resistances are essential to lower the noise figure. According to these results, HEMTs with a shorter gate length and a lower source resistance than the previous ones, were fabricated by using the self-aligned gate technique.

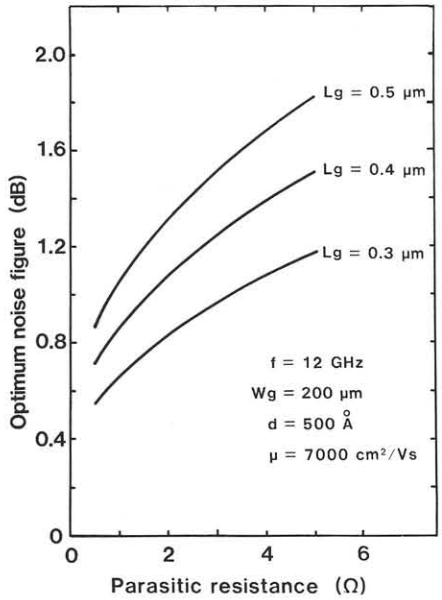
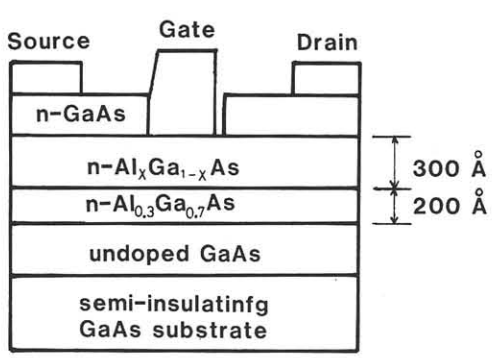


Fig. 1 Calculated optimum noise figure as a function of parasitic resistance for gate length of 0.3 μm, 0.4 μm and 0.5 μm.

3. Device fabrication

The epitaxial layers for HEMTs were grown by molecular beam epitaxy. The layers consist of undoped GaAs, Si-doped n-type AlGaAs, n-type AlGaAs with the mole fraction of AlAs gradually changed, and n-type GaAs, on 2-inch diameter semi-insulated GaAs wafer. The doping concentration is $2 \times 10^{18}/cm^3$. Growth temperature is 680°C. To reduce the ohmic contact resistance, the n-GaAs cap layer was added. The gradually changed AlGaAs layer was grown to eliminate the discontinuity in the conduction band between n-AlGaAs and n-GaAs, and to obtain low source resistance. Hall mobility of the 2-dimensional electron gas was about 6000 $cm^2/V \cdot s$ at room temperature. Undoped AlGaAs " spacer layer " was not grown in the heterojunction, to obtain as high sheet carrier density and low sheet resistance as possible. This structure was adopted to produce a HEMT with a low noise figure at room temperature.



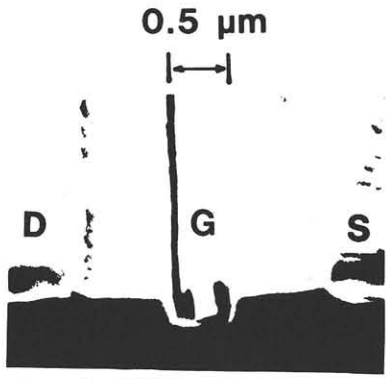


Fig. 2 Cross-sectional view of self-aligned gate HEMT.

HEMTs were fabricated with 0.4 μm gate length and 200 μm total gate width. The channel length between source and drain contacts is 1.6 μm. Fabrication process is simple. To isolate the mesa, Si-doped n-type layers were wet-chemical etched. Source-drain contact areas were defined by photolithography. Ohmic metals AuGe/Au were lifted off and alloyed at 450 ℃. It is confirmed that the alloyed region reaches to the buried 2DEG. Gate areas were delineated by direct electron beam lithography.

To make the self-aligned gate structure (Fig. 2), the anisotropic dry etching technique with vertical wall character was used. The GaAs cap layer of the gate region is selectively removed by this technique. Using the mask resist of the dry etching process, evaporated Al gate metal was lifted off. Since the gate metal and the n-GaAs layer were self-aligned, the source resistance was reduced from 4 Ω to 2.5 Ω. Patterned gate length is 0.5 μm but angled evaporation of Al reduced the device gate length to about 0.4 μm. The etching gas is composed of CCl_2F_2 and He. The dry etching process is essentially a self-terminated one. The uniformity of the pinch-off voltage (-2.0 V) is excellent. We have not found any significant damage to the 2DEG.

4. Performance

The drain I-V characteristics of the HEMT are shown in Fig. 3. Because of the conduction of the low mobility electrons in the AlGaAs layer, the transconductance was low at low gate voltages. The maximum transconductance was 40 mS, that is 200 mS/mm gate width.

For microwave evaluation, HEMT chips were

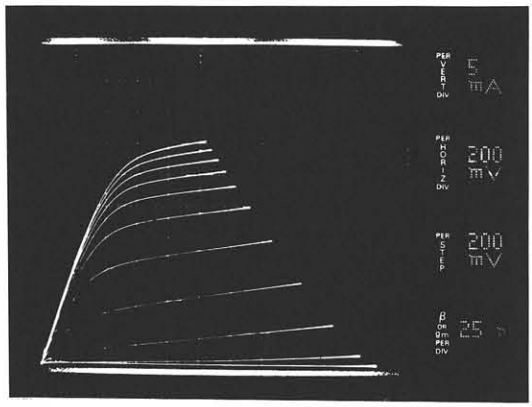


Fig. 3 Drain I-V characteristics.

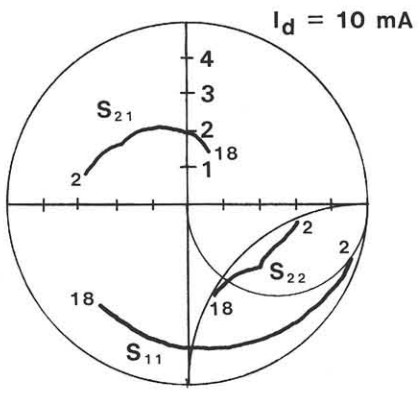


Fig. 4 S-parameters of self-aligned gate HEMT.

mounted on carriers with 0.38 mm alumina microstrip input and output transmission lines, which were slid into a test fixture. The S-parameters were measured over a 2-18 GHz frequency range, using an automatic network analyzer. Fig. 4 shows S-parameters at 10 mA drain current. The small phase rotation of S_{11} indicates small gate capacitance corresponding to the low transconductance. These S-parameters were then used to determine the maximum available gain, the current gain, and the equivalent circuit element values.

Noise figures were measured at 12 GHz and 19.6 GHz. Tuning was done by gold chips along the 50 Ω input and output lines of the carrier. Fig. 5 shows the drain current dependence of minimum noise figure and associated gain at 19.6 GHz. Extremely low noise figure and high gain was obtained at samll drain current. 1.08 dB noise figure with 12.7 dB associated gain at 12 GHz and 1.7 dB noise figure with 8.8 dB associated gain at 19.6 GHz were obtained. Fig. 6 shows the measured noise figure and the frequency dependence of the calculated noise figure for parasitic resistances of 4 Ω, 1 Ω and 0 Ω.

Table 1 summarizes the device parameters and the noise performance of the HEMTs with 0.4 μm and 0.5 μm gate length. In spite of longer gate length HEMTs exhibit noise figures comparable to the best data for quarter-micron gate GaAs MESFET. With further reduction of gate length and source resistance, further improvement of noise performance can be expected.

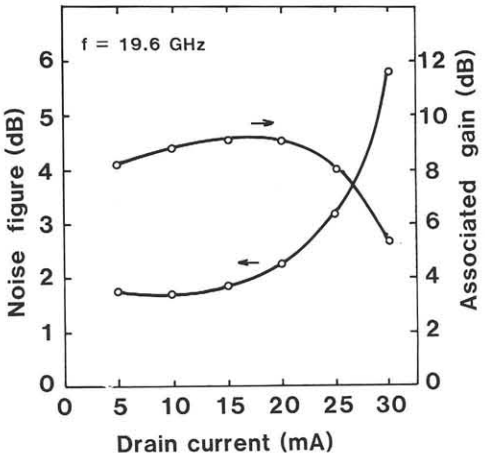


Fig. 5 Minimum noise figure and associated gain as a function of drain current.

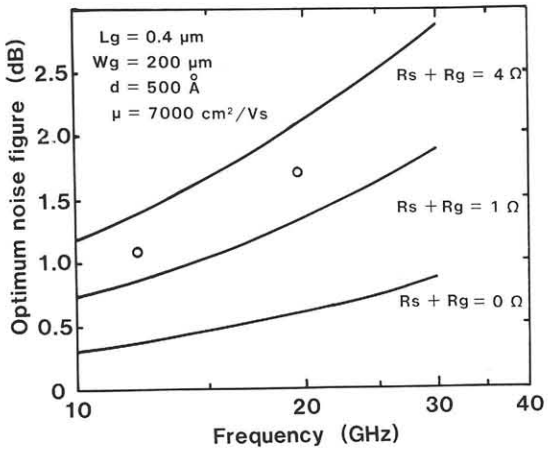


Fig. 6 Optimum noise figure as a function of frequency. —— Calculated noise figure for parasitic resistances of 4 Ω, 1 Ω and 0 Ω. o Measured noise figure.

	Lg (μm)	Rs (Ω)	Fo (dB) (12 GHz)	Fo (dB) (19.6 GHz)
wet-recessed gate	0.5	4.0	1.4	2.2
self-aligned gate	0.4	2.5	1.08	1.7

Table 1 Summary of device parameters and noise performance of self-aligned gate HEMT.

5. Conclusion

High electron mobility transistors with self-aligned gate structure have been developed. With the reduced gate length and source resistance, HEMT exhibited 1.08 dB noise figure with 12.7 dB associated gain at 12 GHz, and 1.7 dB noise figure with 8.8 dB associated gain at 19.6 GHz. These results show the great potential of HEMTs for low noise application.

Acknowledgment

The authors thank M. Kobayashi, A. Shibatomi, S. Yamamoto, Y. Tokumitsu, and H. Ishiwari for their support in this work. They are also grateful to M. Nunokawa for his assistance in fabricating the devices.

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