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A New GaAs HJFET DCFL with Increased Logic Swing

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We propose a new GaAs DCFL using an HJFET[1]-driver/MESFET-load inverter, where a twice larger logic swing than that in the conventional MESFET DCFL has been obtained. The new inverter consists of the HJFET driver and the MESFET load which are formed on a single MBE-grown active layer. The difference of the built-in voltage between hetero- and Schottky-junctions permits normally-off and normally-on operations for the drivers and for the loads, respectively. Design consideration, fabrication process and experiment results are described in full detail.

§1. Introduction

GaAs LSI's have recently attracted much interest with respect to very high speed applications. GaAs LSI's were first initiated by circuit configulations using normally-on FET's. For larger scale integration, the direct coupled FET logic (DCFL) using normally-off FET's is desired because of its low dissipation power and simple circuitry. The DCFL, however, possesses inherent drawback that the logic swing is limited to such a small values as about 0.7 V which corresponds to the built-in voltage of the Schottky-junction. This means that the precise control of the threshold voltages of the consituent FET's on the entire wafer is required.

In this paper, we propose a new GaAs DCFL that provides twice larger logic swing than that in the conventional GaAs DCFL.

§2. Inverter configuration -- A new HJFET/MESFET inverter

Figure 1 shows a schematic drawing of the new inverter. It is noted that a normally-off Hetero JFET (HJFET) driver and a normally-on MESFET load are formed on a single active layer by making successful use of the difference of the built-in voltage between hetero- and Schottky-junctions. As will be discussed later, the built-in voltage of the active FET with the Hetero-junction is almost twice larger than that of the

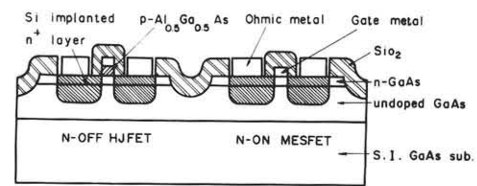

Fig. 1 Schematic drawing of the new inverter.

load FET with the Schottky-junction so that both normally-off and -on FET's can be formed on a single active layer.

§3. Design consideration

An essential point to be considered for integrating the normally-off HJFET's and the normally-on MESFET's on a single active layer is to determine the carrier concentration N and the thickness a of the epitaxial layer.

A threshold voltage V_T of the FET is generally given as a difference between the built-in voltage V_{bi} and the pinch-off voltage V_p accompanying following equations.

$$V_{TH} = V_{biH} - V_{pH} \quad (1)$$

$$V_{TM} = V_{biM} - V_{pM} \quad (2)$$

where subscript H and M represent the MESFET and the HJFET, respectively. Since the pinch-off voltage is given by

$$V_{pH} = V_{pM} = q N_D a^2/2\varepsilon \quad (3)$$

Eq. (1) and Eq. (2) become

$$V_{TH} = V_{biH} - q\, N_D a^2/2\varepsilon \quad (4)$$

$$V_{TM} = V_{biM} - q\, N_D a^2/2\varepsilon\, . \quad (5)$$

N_D is the net donor concentration in the active layer. ε is the permitivity of GaAs.

The built-in voltage V_{biH} of p-$Al_{0.5}Ga_{0.5}As$ /n-GaAs hetero-junction is calculated as

$$V_{biH} = \frac{\varepsilon gp - \Delta\varepsilon c}{q} - \frac{kT}{q} \ln \frac{N_{cn}}{N_A} \frac{N_{vp}}{N_D} \quad . (6)$$

ε_{gp} is the band gap of the p-$Al_{0.5}Ga_{0.5}As$. $\Delta\varepsilon_c$ is the conduction band discontinuity. N_{cn} and N_{vp} are the effective density of states in the conduction band of GaAs and in the valence band of $Al_{0.5}Ga_{0.5}As$, respectively. N_A and N_D are net acceptor concentration in the p-$Al_{0.5}Ga_{0.5}As$ layer and the net donor concentration in the GaAs layer, respectively.

The built-in voltage V_{biM} of the Schottky-junction is calculated as

$$V_{biM} = \Phi_{Bn} - \frac{kT}{q} \ln \frac{N_{cn}}{N_D} \quad (7)$$

where Φ_{Bn} is a barrier height of the Schottky-junction. In the present study where we use TaWSi as Schottky-metal, Φ_{Bn} is measured to be 0.67 eV from the I-V characteristics.

Insertion of Eq. (6) and Eq. (7) into Eq. (4) and Eq. (5) yields

$$V_{TH} = \frac{\varepsilon gp - \Delta\varepsilon c}{q} - \frac{kT}{q} \ln \frac{N_{cn} N_{vp}}{N_A N_D} - \frac{qN_D a^2}{2\varepsilon} \quad (8)$$

$$V_{TM} = \Phi_{Bn} - \frac{kT}{q} \ln \frac{N_{cn}}{N_D} - \frac{qN_D a^2}{2\varepsilon} \quad . \quad (9)$$

The threshold voltage of a normally-on MESFET V_{TM} is negative and that of a normally-off HJFET V_{TH} is positive, so that we have

$$\frac{\varepsilon gp - \Delta\varepsilon c}{q} - \frac{kT}{q} \ln \frac{N_{cn} N_{vp}}{N_A N_D} - \frac{qN_D a^2}{2\varepsilon} > 0 \quad (10)$$

$$\Phi_{Bn} - \frac{kT}{q} \ln \frac{N_{cn}}{N_D} - \frac{qN_D a^2}{2\varepsilon} < 0 \quad . \quad (11)$$

The present new HJFET/MESFET inverter can operate so long as Eq. (10) and Eq. (11) are satisfied. In another word, Eq. (10) and Eq. (11) are necessary conditions that allow integration of normally-on and -off FET's on a single active layer. Numerically calculated results of Eq. (10) and Eq. (11) are shown in Figure 2 where we may find allowable ranges for N_D and a. Constants used for the calculation are listed in Table 1.

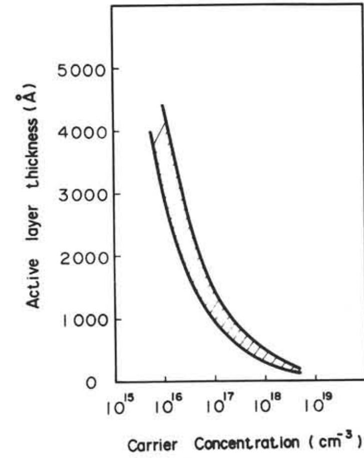

Fig. 2 Allowable range for N_D and a of a single active layer.

εgp	1.95 eV
$\Delta\varepsilon c$	0.46 eV
Ncn	4.7×10^{17} cm^{-3}
Nvp	6.79×10^{18} cm^{-3}
NA	1×10^{18} cm^{-3}
ε	1.17×10^{-12} F/cm
k	1.38×10^{16} erg/K
T	300 K
q	1.6×10^{-19} C

Table 1 Constants used for the calculation.

§4. Fabrication

According to the above design consideration, the carrier concentration N_D and the thickness a of the epitaxial layer were determined to be 1×10^{17} cm^{-3} and 0.13 μm for the experimental device.

Figure 3 shows major steps of the fabrication processes for the new HJFET/MESFET inverter.

Step 1 ; four layers were successively grown by MBE on a LEC-grown undoped semi-insulating substrate, a 2.0 μm thick undoped GaAs buffer layer, a 0.13 μm thick n-GaAs ($N_D = 1 \times 10^{17}$ cm^{-3}) active layer, a 0.2 μm thick p-$Al_{0.5}Ga_{0.5}As$ ($N_A = 1 \times 10^{18}$ cm^{-3}) gate layer and a 0.02 μm p-GaAs ($N_A = 2 \times 10^{18}$ cm^{-3}) contact layer. Silicon and Beryllium were used for the n-type and the p-type dopant, respectively.

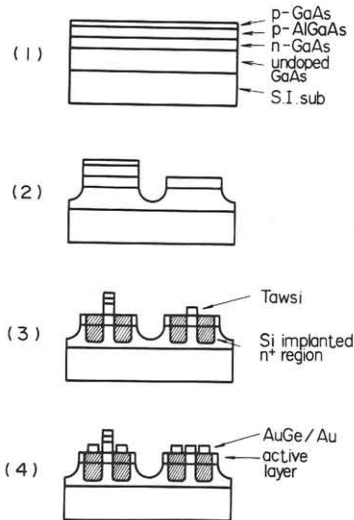

Fig. 3 Major steps of the fabrication processes.

Step 2 ; the active region of the FET was defined by mesa-etching. p-$Al_{0.5}Ga_{0.5}As$ layer on the active region of the MESFET was selectively removed by use of iodine solution(2), KI : I_2 : H_2O = 7 g : 4 g : 177 g. The etching rate of this etchant at 20 °C was 11 μm/min for $Al_{0.5}Ga_{0.5}As$ and 0.01 μm/min for GaAs. Under this condition, etcing of $Al_{0.5}Ga_{0.5}As$ automatically stopped at the interface. Therefore, the precisely controlled MBE active layer thickness was maintained even after the p-$Al_{0.5}Ga_{0.5}As$ layer was etched off.

Step 3 ; a 0.2 μm thick TaWSi film was deposited by RF sputtering. The weight composition of the Schottky-gate metal was Ta : W : Si = 15 : 75 : 10. The gate electrodes were formed by CF_4 + O_2 plasma etching. Self-aligned n^+-regions were made by $^{29}Si^+$ implantation at 150 keV with a dose of 5 x 10^{13} cm^{-2}. Annealing was carried out at 800 °C for 10 minutes in N_2 ambient gas with a SiO_2 encapsulation film. The TaWSi Schottky-gate was extremely stable even after annealing at 800 °C. Figure 4 shows the barrier height Φ_{Bn} and the ideality factor n as functions of annealing time at 800 °C. as shown in Figure 4, Φ_{Bn} is 0.67 eV and n is better than 1.2.

Step 4 ; a AuGe/Au film was evaporated and lifed off for the source/drain electrodes. Alloying was performed at 500 °C in H_2 ambient gas.

§5. Results and discussion

DC characteristics of the normally-off HJFET and the normally-on MESFET with the same geometry (W/L = 10 μm/2 μm) are shown in Figure 5 and Figure 6. The threshold voltage V_{TH} of the HJFET and V_{TM} of the MESFET are 0.1 V and -0.6 V, respectively. It is noted that this result is quite agreeable with the design consideration discussed previously.

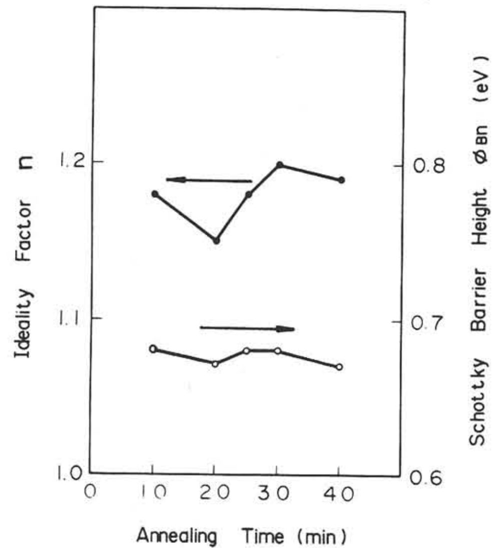

Fig. 4 The barrier height and the ideality factor as functions of annealing time at 800 °C.

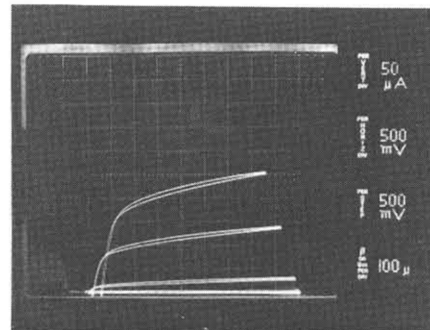

Fig. 5 DC characteristics of the normally-off HJFET.

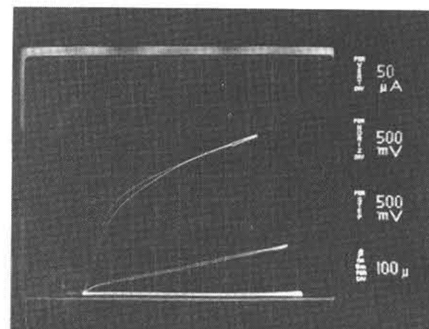

Fig. 6 DC characteristics of the normally-on MESFET.

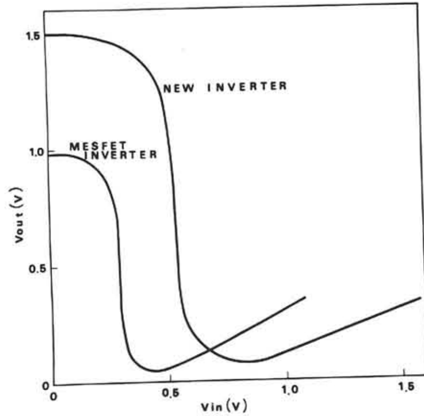

Fig. 7 DC transfer characteristics of the new inverter and the MESFET inverter.

DC transfer characteristics of the new inverter is shown in Figure 7, comparing with that of the conventional MESFET inverter with the same geometry; W/L = 40 μm/2 μm for the driver, W/L = 10 μm/2 μm for the load. As can be seen in this figure, the logic swing of the new inverter is about 1.4 V which is almost twice larger than that of the conventional MESFET inverter.

It is noteworthy that current drive capability of the HJFET is larger than that of a MESFET in terms of the maximum drain to source current $I_{DS\,max}$. We now assume the same geometry, the same threshold voltage V_T and the same carrier concentration N_D between the HJFET and the MESFET. Then the maximum drain to source currents $I_{DS\,max}$ for both FET's can be given as

$$I_{DSH\,max} = \frac{K}{a_H} (V_T - V_{GH\,max})^2 \qquad (12)$$

$$I_{DSM\,max} = \frac{K}{a_M} (V_T - V_{GM\,max})^2 \qquad (13)$$

where subscript H and M represent HJFET and MESFET. K is a constant depending on a geometry. $V_{GH\,max}$ and $V_{GM\,max}$ are the maximum gate bias for both FET's. Deviding Eq. (12) by Eq. (13), we have

$$I_{DSH\,max}/I_{DSM\,max} = \frac{a_M}{a_H}\left(\frac{V_T - V_{GH\,max}}{V_T - V_{GM\,max}}\right)^2 \qquad (14)$$

where a_M and a_H are thickness of the active layer of both FET's. a_M and a_H are

$$a_H = \sqrt{2\varepsilon(V_{biH} - V_T)/qN_D} \qquad (15)$$

$$a_M = \sqrt{2\varepsilon(V_{biM} - V_T)/qN_D} \quad . \qquad (16)$$

Inserting Eq. (15) and Eq. (16) into Eq. (14) yields

$$\frac{I_{DSH\,max}}{I_{DSM\,max}} = \sqrt{\frac{V_{biM} - V_T}{V_{biH} - V_T}}\left(\frac{V_T - V_{GH\,max}}{V_T - V_{GM\,max}}\right)^2 . \qquad (17)$$

We now use the values of 0.63 V and 1.4 V for V_{biM} and V_{biH} respectively, as discussed previously. From Figure 7, $V_{GH\,max}$ and $V_{GM\,max}$ which correspond maximum logic swings of both inverters are determined to be 1.4 V and 0.7 V, respectively. Inserting these constants and V_T = 0.1 V into Eq. (7) yields

$$\frac{I_{DSH\,max}}{I_{DSM\,max}} = 3.0 \quad . \qquad (18)$$

This result shows that the current driving capability of the HJFET is three-times larger than that of the MESFET. It is obvious that this larger driving capability is also advantageous for high speed operations of the LSI's.

§6. Conclusion

The new GaAs HJFET DCFL has been demonstrated. This new DCFL has almost twice larger logic swing than that in the conventional MESFET DCFL. This advantage would be quite attractive for further efforts to GaAs LSI implementation.

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