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Invited

HEMT LSI Circuits

M. Abe, T. Mimura, K. Nishiuchi, A. Shibatomi and M. Kobayashi

Fujitsu Laboratories Ltd., Fujitsu Limited

1677, Ono, Atsugi 243-01, Japan

Self-aligned High Electron Mobility Transistor (HEMT) technology based on selectively doped GaAs/AlGaAs heterojunction structure for LSI circuits is described. Internal logic delay of 22 ps per gate at 77K was achieved at a fan-out of about 2, roughly three times faster than that of GaAs MESFET technology. HEMT 1Kb and 4Kb sRAM circuits have been successfully developed. HEMT 1Kb sRAM demonstrated address access time of 0.87 ns with power dissipation of 360 mW at 77K. Projected performance of HEMT 4Kb sRAM is sub-ns address access time using 1 μm gate device and 2 μm line process technology.

I. Introduction

The information processing in 1990 will need ultra-high-speed computers, requiring high speed LSI circuits with logic delays of sub-100 ps.[1,2]

High Electron Mobility Transistor (HEMT) technology has opened the door on new possibilities for ultra-high-speed LSI/VLSI applications.[3-6] Due to the super-mobility GaAs/AlGaAs heterojurction structure, HEMT is especially attractive for low temperature operations at liquid nitrogen temperature. In 1981, a HEMT ring oscillator with the gate length of 1.7 μm demonstrated 17.1 ps switching delay with 0.96 mW power dissipation per gate at 77K, indicating that switching delay below 10 ps will be achievable with 1 μm gate devices.[4] Switching delay of 12.2 ps with 1.1 mW power dissipation per gate has already been obtained with 1 μm-gate HEMT at room temperature.[7]

This paper presents the recent advances in HEMT technology for high performance LSI circuits, i.e., self-alignment fabrication technology, HEMT performances, logic and memory LSI circuits.

II. Self-Alignment Fabrication Technology

Figure 1 is a cross-sectional view of a typical self-aligned structure of enhancement-mode (E) and depletion-mode (D) HEMTs forming an inverter for DCFL circuit configuration. The basic epilayer structure consists of a 600 nm undoped GaAs layer, a 30 nm $Al_{0.3}Ga_{0.7}As$ layer doped to 2 x 10^{18} cm^{-3} with Si, and a 70 nm GaAs top layer successively grown on a semi-insulating substrate by MBE. The low field electron mobility was found from Hall measurements to be 7200 $cm^2/V.s$ at 300K and 38000 $cm^2/V.s$ at 77K. The concentration of two Dimensional Electron Gas (2DEG) was 1.0 x 10^{12} cm^{-2} at 300K and 8.4 x 10^{11} cm^{-2} at 77K. A thin $Al_{0.3}Ga_{0.7}As$ layer to act as a stopper against selective dry etching is embedded in the top GaAs layer to fabricate E-and D-HEMTs in the same wafer. By adopting this new device structure, we can apply the selective dry etching of GaAs to AlGaAs to achieve precise control of the gate recessing process for E- and D-HEMTs.

The fabrication of E/D-HEMT circuits starts with etching shallow mesa islands down to the undoped GaAs layer to localize the active region. Next the source and drain for E- and D-HEMTs are metallized with AuGe/Au eutectic alloy to

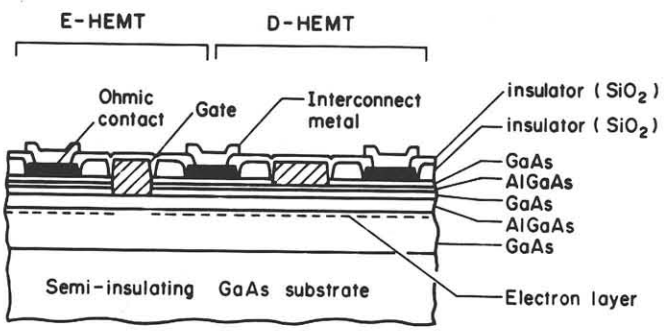

Fig. 1 Cross-sectional view of the self-aligned structure of E/D-HEMTs forming an inverter for DCFL circuit configuration.

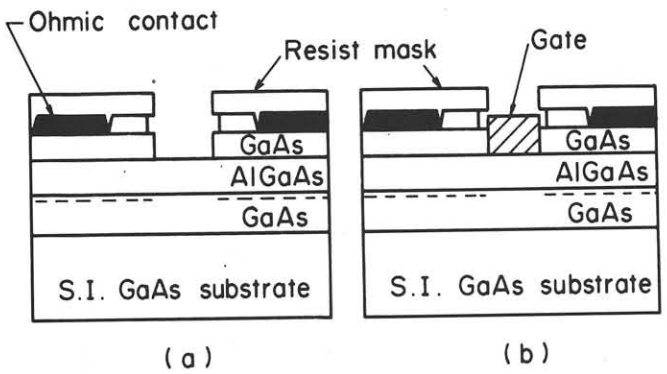

Fig. 2 Self-alignment fabrication: (9) dry recessing of n-GaAs layer, and (b) gate metallization.

form ohmic contact with the 2DEG. Then selective dry etching using an etching gas composed of CCl_2F_2 and He[8] is carried out to remove the GaAs top layer, exposing the top surface of the thin $Al_{0.3}Ga_{0.7}As$ stopper. A significantly high selectivity ratio of more than 260 was achieved at a power density of 0.18 W/cm^2, where the etching rate of GaAs was about 520 nm/min and that of AlGaAs was as low as 2 nm/min.

Figure 2 shows a step in self-aligned gate HEMT fabrication. Both the recessed structure to control the threshold voltage of the devices and the Schottky contact for the gate can be fabricated by using the same resist pattern, as shown in this figure. As a result, the Schottky gate contact and n-GaAs top layer for ohmic contact are self-aligned to achieve high speed performance.

III. HEMT Device Performances

Figure 3 shows the gate length dependence of device characteristics. The values for V_T and K were obtained by fitting the measured drain-current gate-voltage characteristics of the square root of drain-current versus gate-voltage relationship at V_{ds} of 1 V. Dependence of K-factor and transconductance g_m of E-HEMTs on gate length is measured at both 77K and 300K, and K is plotted in Fig. 3. Dashed line indicates L_g^{-1}-dependence of K-factor, estimated from the gradual channel approximation. Below 1 μm gate length at 300K, K-factor drops off from L_g^{-1}-dependence. Velocity saturation effect and parasitic source resistances probably play a significant role in these results. The 0.5 μm-gate E-HEMT at 77K exhibits g_m of

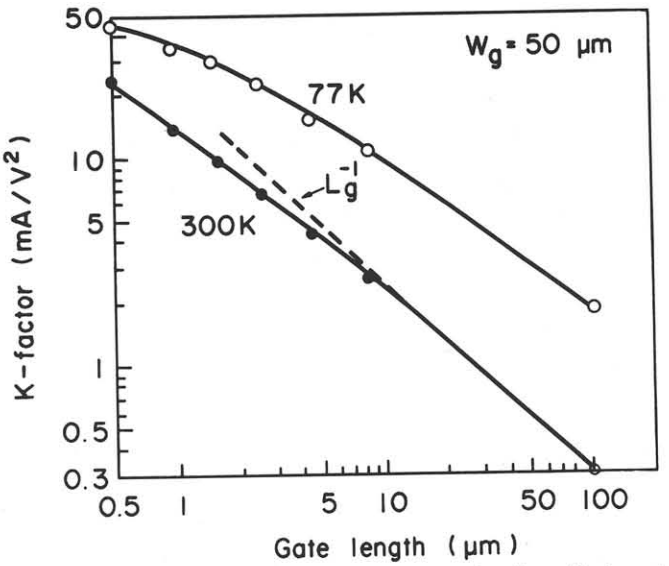

Fig. 3 Dependence of K-factor on gate length Lg at 77K and 300K, respectively.

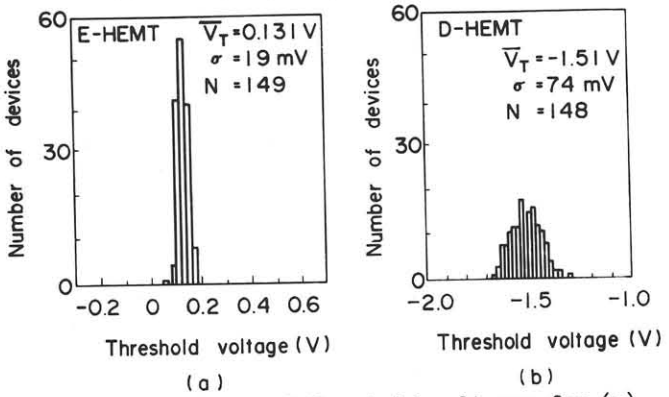

Fig. 4 Histograms of threshold voltages for (a) E-HEMTs and (b) D-HEMTs.

500 mS/mm, which is the highest value ever reported for any FET type device. No significant variation in threshold voltages with gate length was observed in the range from L_g = 10 μm to L_g = 0.5 μm. This indicates that reducing the geometry of HEMTs is an easily acceptable way to increase performance without causing problems regarding short channel effects.

Histograms of threshold uniformities for E- and D-HEMTs are shown in Fig. 4. The standard deviations in threshold voltages, measured for 149 E-HEMTs and 148 D-HEMTs distributed over an area of 15 mm x 30 mm, are 19 mV and 74 mV, respectively. The threshold sensitivity defined by the differential threshold voltage to the thickness of AlGaAs layer can be calculated based on the simple model, to be 70 mV/nm at V_T = 0.13 V. As shown in Fig. 4(a), the deviation in the maximum to minimum threshold voltages for the E-HEMT is 140 mV. This corresponds to a

thickness deviation of only 2 nm over the wafer, indicating excellent controllability of MBE growth and the device fabrication process. The ratio of standard deviation of threshold voltage to the logic voltage swing (0.5 V for DCFL) is 3.8%. This strongly supports the viability of these technologies for realizing ICs with LSI/VLSI level complexities.

IV. Fundamental Logic and LSI Circuits

To evaluate the high speed capability of HEMTs in complex logic circuits, a single-clocked divide-by-two circuit based on the master-slave flip-flop consisting of eight DCFL NOR-gates, one inverter and four output buffers was fabricated. The circuit has a fan-out of up to 3 and 0.5 mm-long interconnects, giving a more meaningful indication of the overall performance of HEMT ICs than that obtained with a simple ring oscillator. The basic gate consists of 0.5 μm x 20 μm-gate E-HEMT and saturated resistors as loads. Divide-by-two operation is demonstrated at up to 8.9 GHz at 77K and up to 5.5 GHz at 300K.[2] The values of 8.9 GHz and 5.5 GHz respectively correspond to internal logic delays per gate of 22 ps with power dissipation of 2.8 mW at 77K, and 36 ps with power dissipation of 2.9 mW at 300K, with an average fan-out of about 2. The speed-power performances of ring oscillators and frequency divider circuits are summarized in Tables I and II. Figure 5 compares switching delay and power dissipation of a variety of frequency dividers.[2,7,10] The switching speed of HEMT is roughly three times as fast as that of GaAs MESFET.

Table I Ring oscillators speed-power performance for HEMT device approaches.

Source (ref)	Approach	Gate length & width (μm x μm)	Switching delay (ps)	Speed-power product (fJ)	Fan-in / Fan-out
Fujitsu (4)	HEMT (77K)	1.7 x 13	17	16	1/1
Fujitsu (2)	HEMT (300K)	0.5 x 20	15	18	1/1
	HEMT (300K)	0.5 x 20	25	4	1/1
Thomson CSF (5)	TEGFET (300K)	0.7 x 20	18	17	1/1
AT & T Bell Lab. (6)	SDHT (77K)	1 x 125	18	141	1/1
	SDHT (300K)	1 x 125	30	135	1/1
Rockwell (7)	HEMT (300K)	1 x 20	12	14	1/1

Table II HEMT frequency divider performance.

Source (ref)	Device approach	Circuit approach	Max. freq. (GHz)	Td (ps)	Pd Td (fJ)
Fujitsu (2)	0.5 μm HEMT (77K)	MS-FF, 1/2	8.9	22	62
	(300K)	(NOR)	5.5	36	104
AT & T Bell Lab. (10)	1 μm SDHT (77K)	D-FF, 1/2	5.9	34	170
	(300K)	(NOR)	3.7	54	173
Rockwell (7)	1 μm HEMT (77K)	D-FF, 1/4	5.2	38	30
	(300K)	(NOR)	3.6	56	26

The HEMT 1K x 1b fully decoded static RAM has been successfully developed with E/D type DCFL circuit configuration.[9] The memory cell is a 6-transistor cross-coupled flip-flop circuit with switching devices having gate lengths of 2.0 μm. For peripheral circuits, a 1.5 μm gate switching device was chosen. In order to obtain high-speed operation, sufficiently high operating current was assigned to peripheral circuits. As a result, peripheral circuits, with 15% of the total device count, dissipate 85% of the chip power. To obtain a good noise margin and guarantee stable logic operation in the HEMT DCFL circuit, which has a small logic swing, special attention was paid to the power supply. The RAM has a total device count of 7244. The design rule for these lines is 3 μm line width and spacing at minimum. Minimum size of the contact hole is 2 μm x 2 μm. The memory cell is 55 μm x 39 μm (2145 μm^2), and the chip size is 3.0 mm x 2.9 mm. Normal read-write operation was confirmed both at 300K and 77K. At 300K, the row address access time was 3.4 ns and chip dissipation power P_{chip} of 290 mW was obtained with a supply voltage V_{dd} of 1.30 V. Sub-nanosecond access operation of access time of 0.87 ns with P_{chip} of 360 mW was achieved with V_{dd} of 1.60 V at 77K. With device parameters designed, HEMT 1Kb static RAMs will achieve sub-500 ps access operation with power dissipation of 1 W.

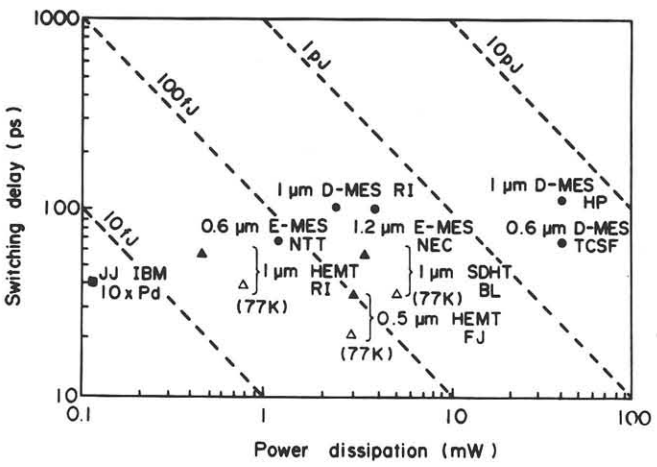

Fig. 5 Switching delay and power dissipation of a variety of frequency dividers. The symbol ● denotes GaAs MESFET at 300K, ▲ and Δ denote HEMTs at 300K and 77K, respectively, and ■ denotes Josephson junction devices.

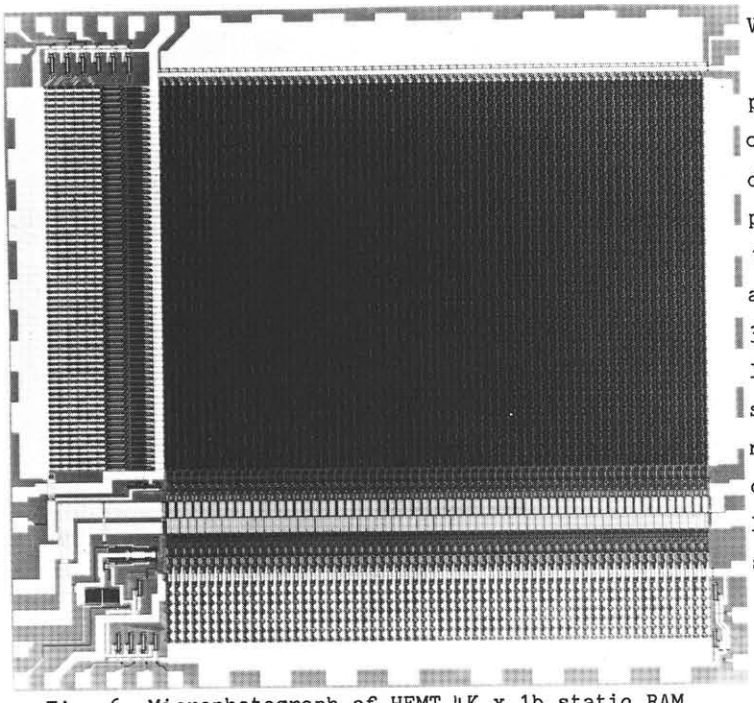

Fig. 6 Microphotograph of HEMT 4K x 1b static RAM, which measures 4.76 mm x 4.35 mm and contains 26864 E/D-HEMTs.

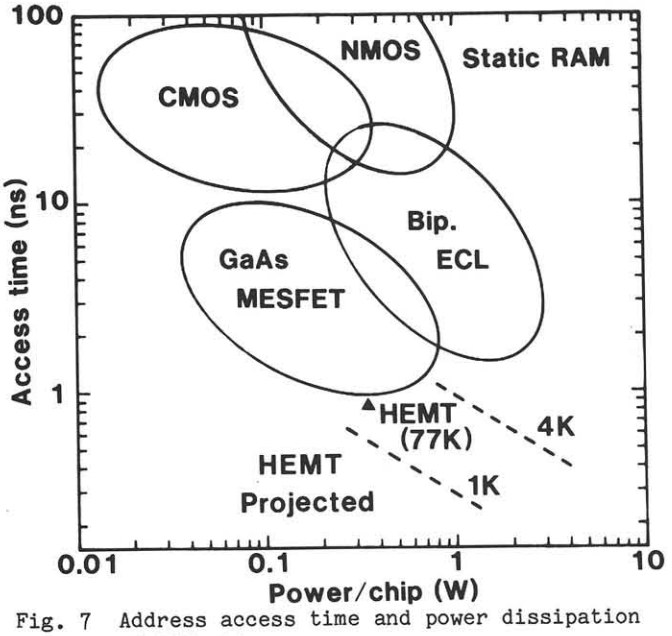

Fig. 7 Address access time and power dissipation of RAM chip.

The HEMT 4K x 1b fully decoded static RAM has also been successfully fabricated using the technology described above, and tested. Figure 6 shows a microphotograph of the 4K x 1b sRAM. The memory cell is 55 μm x 39 μm, the chip is 4.76mm x 4.35 mm, and 26864 HEMTs are integrated in a 4K bit static RAM. Normal read-write operation was confirmed both at 300K and 77K. Figure 7 shows the address access time and power dissipation of sRAM. By using 1-μm gate devices and 2-μm design rule technology, subnanosecond address access time can be projected for the 4Kb sRAM.

V. Summary

Recent advances in HEMT technology for high performance LSI circuits are presented with focus on self alignment fabrication technology using new device structure, controllability in device parameters, logic and memory LSI circuits. A HEMT 1Kb sRAM has been developed to achieve address access time of 0.87 ns with power dissipation of 360 mW at 77K, using 1.5-μm gate devices and 3-μm line process. Under the same technology, HEMT 4Kb sRAM has also been successfully fabricated and normal read-write operation been confirmed. With device technology of 1-μm gate devices and 2-μm line process, HEMT 4Kb sRAM should achieve subnanosecond access operations.

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