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Heterojunction GaAs MIS-Like FET

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A heterojunction GaAs MIS-like FET, in which an n^+-GaAs layer is used as the gate, an undoped GaAlAs layer as the insulator, and an undoped GaAs layer as the semiconductor is reported. The device operated as a normally-off type FET with the threshold voltage of +0.035V, transconductance of 170mS/mm at 77K. The dispersion of the threshold voltage was very small. The device looks therefore very attractive for high-speed large-scale LSI applications.

1. Introduction

HEMTs are very attractive and promissing heterojunction device for high speed LSI applications. A 1K bit static RAM has already been successfully fabricated[1]. In this paper we report another type of heterojunction device which is potentially as good as, or even better than HEMTs for high speed LSI applications.[2]

Our device is a self-aligned accumulation-mode heterojunction GaAs MIS-like FET, in which an n^+-GaAs layer is used as a gate, an undoped GaAlAs layer as an insulator, and an undoped GaAs layer as a semiconductor. We call this device a semiconductor-insulator-semiconductor (SIS) FET, emphasizing the use of an n^+-GaAs layer as a gate. The n^+-GaAs gate is employed in order to obtain the onset of surface accumulation condition at the gate voltage of almost zero. Therefore our SIS FET has the threshold gate voltage of almost zero. The threshold voltage is expected to be very weakly dependent on the thickness of the GaAlAs layer, or on the concentration of the unintentionally doped impurities in the otherwise undoped GaAlAs layer. This will make the fabrication process very easy to obtain FETs of uniform threshold voltages. The self-aligned structure, which is essential for an accumulation-mode FET, and also help reduce the source resistance, is obtained by applying ion implantation technique. This has been made possible by the lack of impurities in the GaAlAs layer

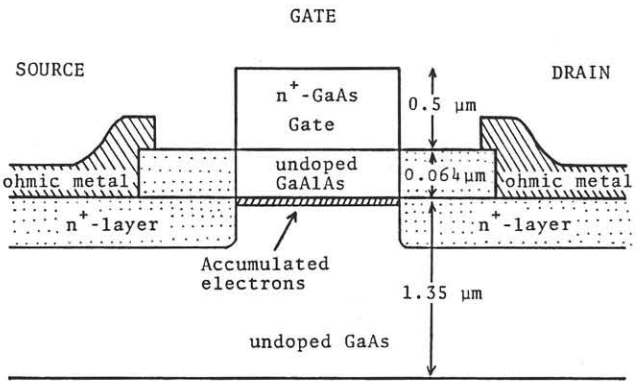

Fig.1 Schematic structure of GaAs MIS-like FET.

(against high-impurity concentration in GaAlAs of HEMTs) which would diffuse into the undoped GaAs during the post-implantation annealling and destroy the high electron mobility there. Moreover, the lack of impurities in GaAlAs gives a higher electron mobility than in a HEMT. The present device has a similar operation mode to that of a Si gate MOSFET.

2. Structure and fabrication process

The structure of a SIS FET is shown in Fig.1. The features of the FET are that 1) the gate electrode is made of n^+-GaAs, 2) an undoped GaAlAs layer is used as the insulator, and 3) a self-alignment structure is employed.

Fig. 2 shows a schematic diagram of the fabrication process of SIS FET.

1) The fabrication process started with the crystal growth of following structure by MBE on an S.I. LEC (100) GaAs substrate : undoped GaAs (1.35μm)/undoped $Ga_{0.6}Al_{0.4}As$ (0.064μm)/n^+-GaAs (Si-doped, $1x10^{18}/cm^3$, 0.5μm). In the Figure, the LEC GaAs substrate is omitted for simplicity.

2) The top n^+-GaAs layer was selectively etched off using a chemical etchant, leaving a strip of 2μm in length and 20μm in width which worked as the gate.

3) Using the n^+-GaAs gate as a mask, $2x10^{13}/cm^2$ Si ions were implanted at 100keV through the GaAlAs layer to form the self-aligned source and drain n^+-regions. The acceleration energy is so selected that the implanted impurity has the peak concentration near at the GaAlAs/undoped GaAs interface. This is to ensure a good contact between the two-dimensional electron gas induced at GaAs/GaAlAs interface and the source and drain n^+-regions. The n^+-GaAs gate is so thick that it can sufficiently protect the invasion of the implanted Si ions into the GaAlAs layer. (The projection range R_p and the standard deviation σ_p of Si in GaAs at E=100keV are R_p=840Å and σ_p=446Å, respectively.)

4) The sample was then annealed in an infra-red lamp furnace at 800°C for 30 seconds without a cap, under an arsenic pressure. The obtained sheet resistance of the n^+-regions is 500Ω/□.

5) After selectively etching the GaAlAs layer, source and drain ohmic contacts, 8μm apart, were formed with Au·Ge/Ni/Au by alloying at 440°C for 1 minutes.

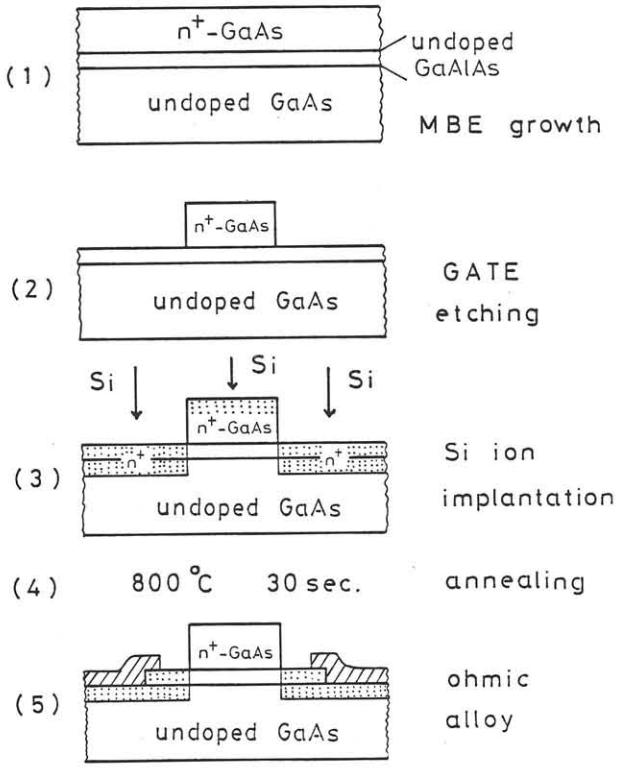

Fig.2 Fabrication process of GaAs MIS-like FET.

3. Device Characteristics

The critical point in the fabrication process is the annealing conditions. The FET must retain the heterojunction MIS structure even after high temperature annealing process. To check this, MIS capacitance-voltage characteristics are measured at 77K in dark using a sample with the structure of n^+-GaAs (Si-doped, $5x10^{17}/cm^3$, 0.4μm)/undoped GaAlAs(750Å)/ n-GaAs(Si-doped, $5x10^{16}/cm^3$, 1μm)/ HB n^+-GaAs substrate as shown in Fig.3 before and after annealing process. Ohmic electrodes are deposited on the top and bottom GaAs layers. The annealing condition is the same as that mentioned in the fabrication process 4).

The measured C-V characteristic are shown in Fig. 4. Though the flat-band voltage shifts from 0V to +0.04V after annealing process, the sample still retain a good MIS C-V characteristic. However, in the case of annealing temperature of above 850 °C, the sample did not show an MIS C-V characterisitic, suggesting a destruction of the MIS structure. The cause of the threshold voltage shift of 0.04V is not clear so far. One of the possible reasons is the diffusion of doped Si in the n^+-GaAs gate into the undoped GaAlAs layer, which leads to the reduction of the effective thickness of the insulator.

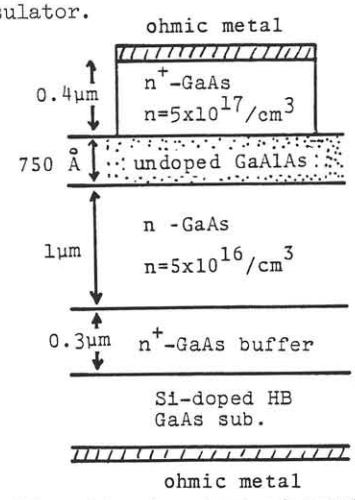

Fig.3 Schematic structure of sample for C-V measurement.

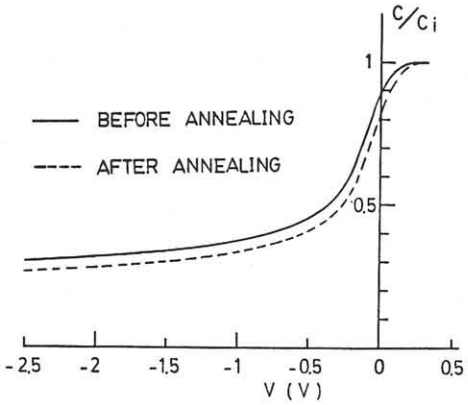

Fig.4 MIS C-V characteristics before and after annealing process.

Fig. 5 shows the capacitance-voltage characteristics between the gate and the source electrodes of the SIS FET at 77K in dark with the drain terminal open. The measured characteristic shows a clear MIS C-V curve, which consists of the accumulation region, the depletion region, and inversion region. The flat-band voltage is small, V_{FB}=+0.16V, as is expected by the use of the n^+-GaAs gate. From the C-V characteristic, the undoped GaAs layer is calculated to be unintentionally doped to $\sim 2.4\times10^{15}/cm^3$ at 77K.

Fig.6 shows the gate/source I-V curve with the drain terminal open at 77K in dark. Strongly rectifying behavior is seen due to the difference between the n^+-GaAs gate and the unintentionally doped GaAs layer[3]. The voltages at which the current exceeded 0.04mA are +0.9V and -1.6V for the positive and negative gate polarities, respectively.

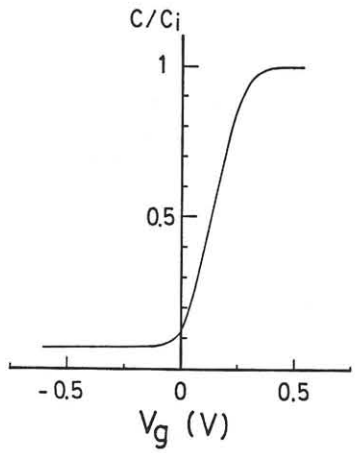

Fig.5 MIS C-V characteristic between gate and source electrodes of MIS-like FET.

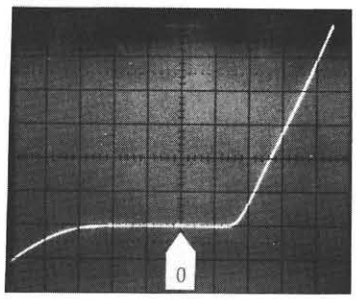

Fig.6 Gate-source I-V curve at 77K in dark. 0.2mA/div, 0.5V/div.

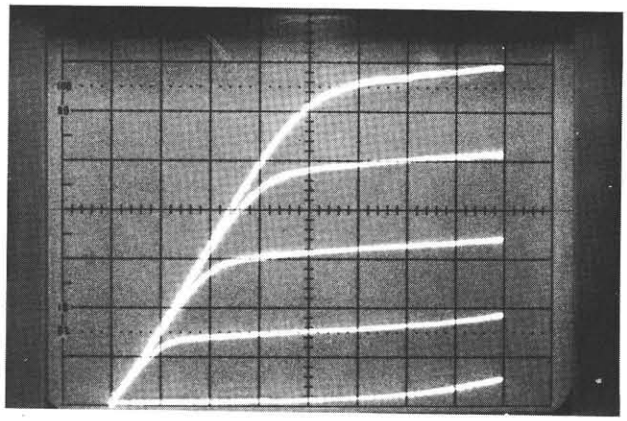

Fig.7 FET characteristics of GaAs MIS-like FET at 77K in dark. 0.4mA/div, 0.2V/div, V_g=0V $\sim$ +0.8V (0.2V step).

The source current I_s vs. drain-source voltage V_{ds} characteristics of a typical SIS FET measured at 77K in dark is shown in Fig.7. The current is almost zero at the gate-source voltage V_g of zero for V_{ds}=1V. The increase of the current with a V_g step is almost constant up to V_g=+0.8V. The gate leak current is negligible up to this gate voltage as shown in Fig.6. The linear dependence of the saturation current on the gate voltage may be due to the velocity saturation of the carrier[4]. The threshold voltage, as determined by the extrapolation of I_s vs. V_g curve at V_{ds}=1V is +0.04V. The transconductance at V_g=+0.8V, V_{ds}=1V is 170mS/mm which is the highest value ever reported on GaAs MIS-like FETs. The drain conductance at the same bias condition is as small as 8mS/mm. Thus the device operates as a normally-off type accumulation-mode FET of high performance.

Though the electron mobility is as high as $40{,}000 cm^2/V \cdot s$, the transconductance of the FET is not so high as was expected. The transconductance is deteriorated by the high source resistance of $\sim$ 150Ω, which is about twice as high as that of a typical self-aligned GaAs FET. The high value of the source resistance is attributed to not-optimized ion-inplantation and annealing conditions.

The threshold voltages of 41 samples extended over a $10 \times 5 mm^2$ wafer were measured. The distribution of the threshold voltage is shown in Fig.8. The average threshold voltage was 0.035V and the dispersion was 0.013V. Thus one of the most significant features of the present FET, the very low sensitivity of the threshold voltage to the material and process was confirmed.

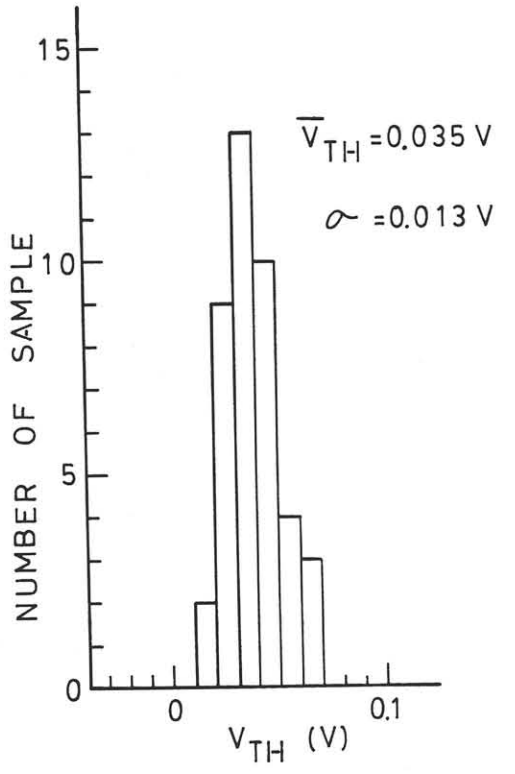

Fig.8 Distribution of threshold voltage of 41 FETs.

4. Conclusion

In conclusion, we fabricated the first self-aligned accumulation-mode GaAs MIS-like FET having an n^+-GaAs/undoped GaAlAs/undoped GaAs structure. We named this device a SIS FET. A typical SIS FET operated at 77K has the threshold voltage of +0.04V, and worked at the gate voltages of up to +0.8V without gate leak current. The measured transconductance was as high as 170mS/mm although the device design was not optimized. The dispersion of the threshold voltages of 41 samples was as low as 0.013V. Since our SIS FET allows the use of ion implantation technique for the fabrication of the self-aligned structure, and since its threshold voltage depends very weekly on the crystals, the device looks very attractive for high-speed high-density logic circuits operating at 77K.

Acknowledgment

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