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Al_2O_3/Native Oxide Double-Layer MIS Structure for InP MISFET IC's

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InP MISFETs with Al_2O_3/native oxide double-layer gate insulators grown by simple anodization processes in electrolyte and in oxygen plasma have been investigated. Device performance was greatly improved by adding thin native oxide intermediate layer, showing effective electron mobilities of 1500 - 3000 $cm^2/V.s$ with marked reduction of the current instability. A mechanism of the current drift was proposed, concerning to usual interface states below semiconductor conduction band edge. Feasibility of the double-layer gate MISFET ICs was also demonstrated by E/D inverters and ring oscillators.

1. Introduction

Compared with currently flourishing GaAs MESFET ICs, MISFET ICs are a more natural extension of the Si technology, and potentially possess several advantages over MESFETs such as larger logic swings and noise margins, larger driving capability, design flexibility, and less severe restriction on substrate uniformity. In addition, various CAD tools developed for Si MOS ICs may be directly applicable to MISFET ICs.

This paper describes InP MISFETs with double-layer gate insulators of Al_2O_3 and native oxide grown by an anodization process of evaporated Al on InP in electrolyte or in oxygen plasma. Both effective mobilities and the current instabilities of the devices are greatly improved by using the double-layer structures. A new understanding of the drift mechanism is also obtained by drift characterization. Finally feasibility of the MISFET ICs is demonstrated by E/D inverters and ring oscillators.

2. MISFET Structure and Fabrication

A cross-sectional view of the fabricated MISFET is schematically shown in Fig. 1. After formation of Au-Ge ohmic contacts, the ion-implanted n^+-layer of the gate region was removed by a selective etching. Al_2O_3/native oxide double-layer was formed by anodizing Al-deposited samples in electrolyte or in oxygen plasma.

For electrolytic anodization, aqueous solution of tartaric acid mixed with propylene glycol (AGW) was used[1]. The anodization was carried out at a constant current density of 0.2 mA/cm^2.

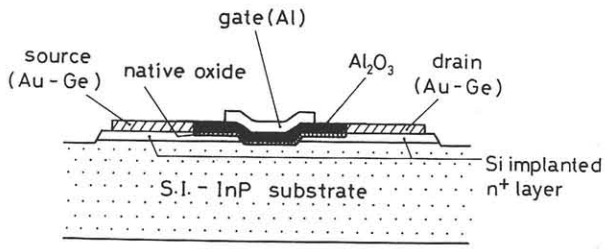

Fig. 1 Cross sectional view of the double-layer MISFET.

Plasma anodization was performed using an oxidation system with a grounded mesh electrode between rf electrode and sample holder[2], thereby avoiding high rates of electron and ion bombardment to the sample. Exciting oxygen plasma by rf power of 20 W at 13.56 MHz, the anodization was initiated by supplying a constant DC current of 0.5 mA/cm^2 to the sample.

Native oxide of InP was formed underneath the Al_2O_3 layer without interrupting anodization in both oxidation processes. The thickness of Al_2O_3 and native oxide were chosen to be in the range of 800 - 1200 Å and 100 - 250 Å, respectively. After Al gate metallization, process was completed by annealing the sample in hydrogen for 30 min.

3. Characterization of MISFET

3.1 Interface States

Figure 2 shows the energy distribution of interface state for annealed samples by Terman's method using 1 MHz C-V curves. Annealing were

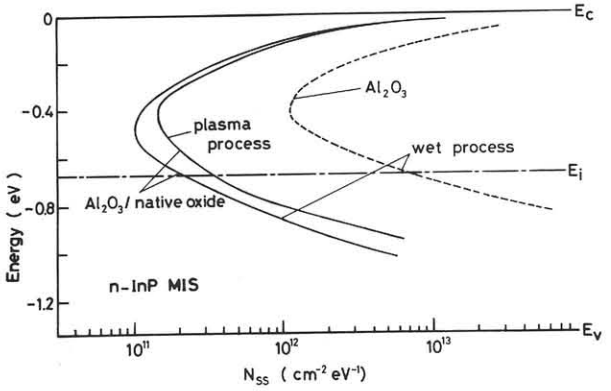

Fig. 2 Energy distribution of interface state density determined by Terman's method.

performed at 400 ℃ for wet-anodized sample and at 300 ℃ for plasma-anodized sample. Curves are U-shaped with minimum values of 9-15 x 10^{10} $cm^{-2}eV^{-1}$ at about 0.4 eV from semiconductor conduction band (E_C) and with 2-4 x $10^{12}cm^{-2}eV^{-1}$ near E_C. These values are about one order magnitude smaller than those of the wet-anodized Al_2O_3 single-layer MIS sample, as shown by dashed line.

3.2 Current-Voltage Characteristics

Figure 3 shows examples of drain current - gate voltage characteristics in the saturation region before and after annealing of devices. For double-layer gate structure, transconductance g_m of 10-12 mS/mm were obtained with 25 μm channel length at a gate bias of 3 V, which corresponds to g_m of 250-300 mS/mm when the channel length is reduced to 1 μm. Using Al_2O_3 single-layer gate structure, typical g_m was 2-4 mS/mm for the same channel length. Effective mobilities μ_{eff}, calculated from the slopes in Fig. 3 and measured insulator capacitances, were typically 1500-3000 $cm^2/V.s$ for double-layer MISFETs with best values of 3050 $cm^2/V.s$ for the wet-anodized process and 3200 $cm^2/V.s$ for plasma-anodized process. On the other hand, μ_{eff} of Al_2O_3 single-layer MISFETs fell in the range of 300-1000 $cm^2/V.s$.

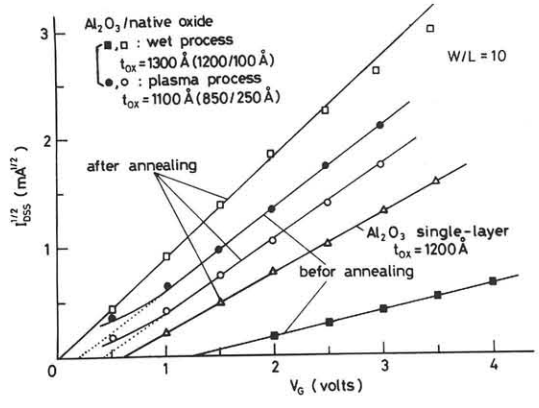

Fig. 3 Square root of drain current vs. gate voltage characteristics of MISFETs in the saturation region.

3.3 Drain Current Stability

Current stability of MISFETs was assessed by recording the change in drain current after application of a gate voltage step under the condition of a constant drain voltage. Figure 4 shows the resultant plots of drain current vs time for the double-layer MISFETs and the single-layer MISFETs, which are normarized at t = 10^{-6} sec. It is seen that decreasing-type current drift is improved by intentionally adding the thin intermediate native oxide layer. The drain current does almost reach its steady state after 10^3 - 10^4 sec. with keeping high current level.

Okamura et al.[3], Lile et al.[4] and Yamaguchi et al.[5] have suggested thermally activated tunneling of electrons into interface states energetically located above E_C to explain the drift phenomena. Wilmsen et al.[6] have supposed that these state are correlated with bulk-like In_2O_3 incorporated into the natural native oxide, whose conduction band is also located slightly above E_C. Here we propose a model where

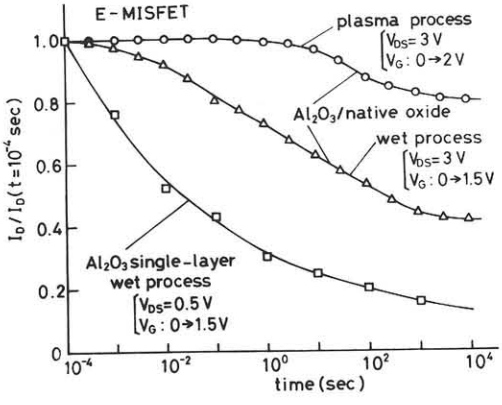

Fig. 4 Normarized drain current vs. time after application of positive gate bias.

energetically and spatially distributed states in the oxide near the interface below E_C of InP are responsible for the present drift.

The temperature dependence of the current drift in the wet-anodized double-layer MISFET is shown in Fig. 5(a), where the drain current drift data were taken by successively lowering the temperature. Previous models shown in Fig. 6(a) and (b) are capable of explaining the strong temperature dependence observed in Fig. 5(a). On the contrary, our model shown in Fig. 6(c), in which capture of electrons through tunneling to the states below E_C in the oxide near the interface is responsible, is not capable of explaining the strong temperature dependence at all. This is because both the capture by lower energy states and the tunneling process are almost temperature independent. Before reaching any conclusion, let us reexamine the experimental data. Since the drift data were taken successively in Fig. 5(a), it is unlikely for the trapped electrons to be reemitted before the next drift experiment, which leads to a non-equilibrium initial condition of state occupation for the next measurement. The number of these occupied states are increased with lowering of temperature due to strong temperature dependence of emission time constant. If this is true the results in Fig. 5(a) arose only from the measurement method, and did not reflect the true physical processes.

When the equilibrium occupancy of the interface state is realized before each drift measurement, almost identical curves of drain current drift should be expected at any temperature, if our model is correct. Figure 5(b) shows such drift curves, where data were taken after holding the device at room temperature for several tens of minutes prior to cooling the device for each drift measurement in order to achieve the equlibrium initial state. It is seen that drift characteristics are unchanged with temperature, which can not be explained by the mechanisms shown in Fig. 6(a) and (b). The results strongly indicates that our model is the correct one. Parallel shift of the current level can be interpreted as additional temperature dependence of the effective mobility and the threshold voltage of the device.

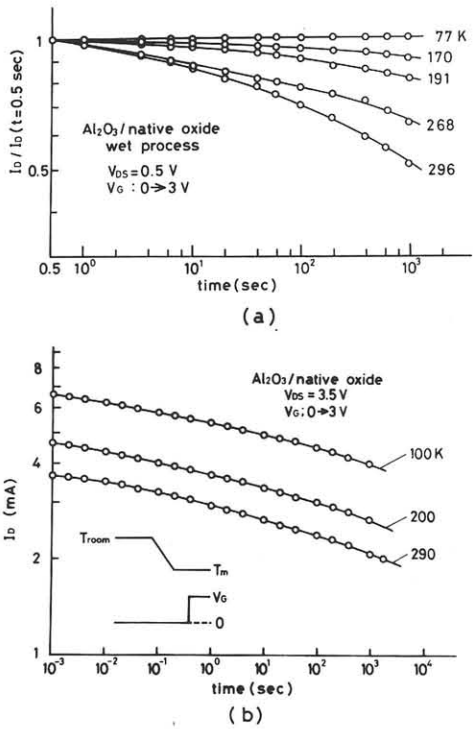

Fig. 5 Difference between temperature dependence of drift curves: data were taken by successively lowering the temperature in (a) and regaining equilibrium at room temperature before each measurement in (b).

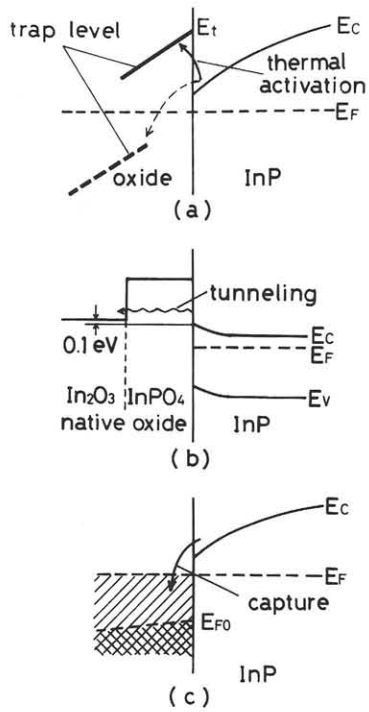

Fig. 6 Schematic band diagram illustrating the current drift: tunneling of thermally excited electrons to (a) interface traps and to (b) conduction band of In_2O_3 native oxide. In (c), capture of electrons by the states under the conduction band through tunneling is illustrated.

Recently, similar mechanism of the drift has been given by Staa et al.[7] based on CCDLTS measurements of MIS capacitors.

4. MISFET Logic

Enhancement-depletion (E/D) type InP MISFET inverters and 7-stage ring oscillators, as shown in Fig. 7, were fabricated using the electrolytic anodization, in order to demonstrate the feasibility of the process. Fabrication process was almost the same as the MISFET except for controlled gate etching in D-FET. Figure 8(a) shows the transfer characteristics of the inverter with the corresponding circuit diagram. Inverter characteristics were stable down to the measured lowest frequency of 10^{-2} Hz. This low-frequency stability of the inverter is greatly superior to GaAs MOSFET inverters[8] as seen from Fig. 8(b). It is consistent with the drastically reduced drain current instability in the present double-layer gate MISFETs. The ring oscillator with channel lengths of 5 μm for E-FET and 20 μm for D-FET showed propagation deley per gate t_{pd} = 4 ns with power-delay product $P.t_{pd}$ = 7 pJ at V_{DD} = 3 V at 128 K. The propagation delay is limited at present by relatively large gate metalization length of 15 μm in E-FET, which is indicated by a circuit simulation. The propagation delay of 4 ns scales down to 40 ps for 1 μm gate metalization length. Present successful operation of the ring oscillator as well as the inverter indicates great potential of the double-layer gate InP MISFET for LSI/VLSI applications.

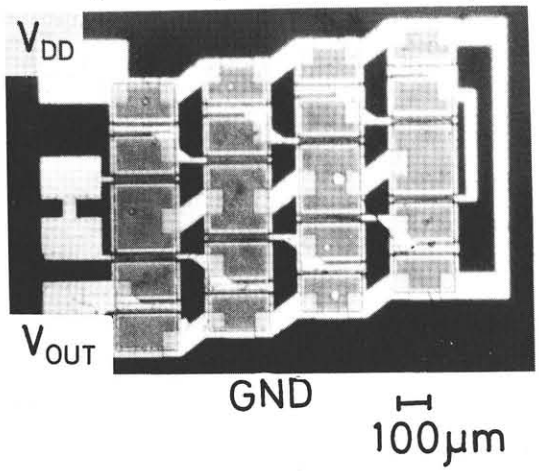

Fig. 7 Photograph of a fabricated 7-stage ring oscillator.

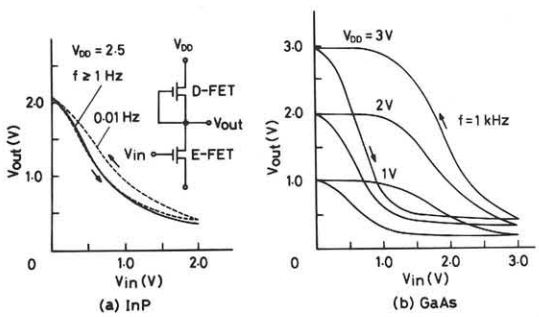

Fig. 8 Comparison of transfer characteristics between (a) InP E/D-MISFET inverter and (b) reported GaAs E/D-MOSFET inverter[8].

5. Summary

Fabrication and characterization of InP MISFET and circuits with double-layer gate insulators, grown by simple anodization processes in electrolyte and in oxygen plasma, was described. Insertion of thin anodized native oxide intermediate layer greatly improved device performance. Effective electron mobilities as high as 1500 - 3000 $cm^2/V.s$ and marked reduction of the current instability were simultaneously achieved. A mechanism of the current drift was given, in which the drift is explained in terms of states near the interface in the oxide below semiconductor conduction band edge. Feasibility of the double-layer gate MISFET ICs was demonstrated by successful fabrication of E/D inverters and ring oscillators.

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