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GaAs MESFET's with a Highly Doped Channel

K.Heime, H.Dämbkes, W.Brockerhoff Solid State Electronic Department, Duisburg University Kommandantenstr. 60, D-4100 Duisburg, FRG

The reduction of the gate length L of FETs into the submicron region gives rise to negative short channel effects unless the channel thickness a is reduced accordingly such that $L/a \gg 1$. For keeping the threshold voltage constant it is necessary to increase the channel doping $N_D \sim 1/a^2$. In this paper it is shown by numerical simulations and experiments that doping concentrations up to $1.3 \cdot 10^{10}$ cm⁻³ can successfully be used for GaAs MESFETs. Optimum concentrations are calculated for which short channel effects are eliminated and simultaneously transconductance and cut-off frequency maximized. Good correlation is found with experimental results. Following the outlined rules the "simple" design rules – used for discrete MESFETs and especially for integrated circuit layout – will remain valid in the submicron region.

1. Introduction

GaAs based devices are in a stage which enables the fabrication of digital LSIs, MMICs and high performance microwave devices. GaAs MESFETs with submicron gates /1/ and channels /2/ are fabricated, resulting in operational frequencies up to 60GHz /3/ and switching times of less than 20ps /4/. But as the lateral dimensions shrink below 1um new problems arise which tend to suppress the expected improvements. Besides technology improvements there is an impetus for modifications in the design of FETs with submicron dimensions. For homogenously doped GaAs MESFETs two major approaches are currently persued: One tends to reduce the channel doping as far as possible, taking advantage of the improved electron dynamics (high mobility. velocity overshoot and possible ballistic effects (5/), while the other tends to increase the channel doping $\mathrm{N}_{_{\mbox{\scriptsize D}}}$ up to concentrations above those used nowadays /6,7,8,9,10/.

Conventional FETs with submicron gates suffer from negative short channel effects. Moreover their current driving capability is restricted and they are inherently more sensitive to interconnection capacitances. Nearly all these difficulties may be overcome by use of high doping concentrations. The negative short channel effects are outlined especially with respect to IC applications. The results of theoretical work and of experiments for GaAs MESFETs with highly doped channels are

described /11,12/.

2. Short Channel Effects

To exploit the good properties inherent in GaAs MESFETs, the extrinsic parasitic elements have to be avoided as far as possible. This is done by use of the recessed-gate structure /e.g.2/ or by deep ion implantation into the extrinsic channel /13/. Thus sheet resistances as low as $100\Omega/\Box$ are achieved. These values are about ten times lower than those in the channel of the intrinsic ungated FET. However with reduction of the gate length L to 1µm or less and maintaining N_D constant (about 10^{17} cm^{-3}) the short-channel effects become effective:

- 1. The threshold voltage ${\rm V}^{}_{\rm T}$ depends on L.
- 2. V_{T} becomes bias dependent.
- The DC-characteristics show no real saturation, hence the output conductance g_d increases with decreasing L and reduces the voltage gain.
- 4. The transconductance g_m tends to saturate /14/ or may even show a "compression" /15/.

Thus the design rules for FET's and IC's have to be adapted to each individual FET if different gate lengths are used. A quantitatively correct design is therefore more difficult as not only doping concentration and layer thickness but also gate length and bias point have to be considered. The velocity overshoot of carriers in the high-field gate region increases current, transconductance and frequency limits /16/. The reason for the short-channel effects is the fact that the ratio of gate length L to channel thickness a is no longer much larger than 1, if with shrinking gate length N_D and the channel thickness a are held constant. In this case the two-dimensional potential and current distributions have to be considered. Especially the electrical field pattern will be influenced by the drain potential, which lowers the barrier in the channel created by the gate potential, resulting in pronounced changes of g_d and V_T /17/. It will be shown that short-channel effects may be diminished if a is reduced and simultaneously N_D increased such that ${\rm V}_{\rm T}$ remains constant. For this purpose GaAs MESFET's with L=0.4+1.2µm and $N_{D}=0.1\pm1.3\cdot10^{18}$ cm⁻³ were made and investigated. In addition computer simulations were performed. The results demonstrate not only that GaAs MESFETs with very high doping concentrations in the channel are feasible but that the short-channel effects are avoidable and that considerable improvements in transconductance and frequency limits are achievable with optimized dopant concentrations /11,12/.

3. Device Technology

The layers were made by LPE, MBE and diffusion /18/. Submicron gates were made by angled evaporation /19/. AuGe/Ni served as ohmic and Cr/Au $(L \ge 1\mu m)$ or Al $(L < 1\mu m)$ as Schottky contacts. Mobility, dopant concentrations, contact and sheet resistances and FET DC properties were measured using a diagnostic pattern. Microwave and noise measurements (2-12GHz) were performed on T-shaped FET's.

4. Theory and Numerical Simulation

The "nominal" threshold voltage is defined as:

$$V_{\text{Tnom}} = V_{\text{bi}} - \sqrt{qN_{\text{D}}a^2/(2\epsilon_{\text{r}}\epsilon_{\text{o}})}$$
(1)

 $(V_{bi} = built-in potential)$. Short-channel effects are not effective if L/a > 3. If a depletion-type MESFET with $V_{Tnom} = -1.2V$ is chosen a channel thickness a < 0.1µm (a=0.05µm in the following example) is necessary for L=0.3µm. From eq.(1) a dopant concentration $N_{D}=10^{18} \text{ cm}^{-3}$ is de-

duced. Such high concentrations have not been used in FET's until now.

The well-known analytic solutions for the FET I-V-characteristics can no longer be used for the short channel because they

- (a) do not include the two-dimensional potential and current distributions
- (b) do not consider the transient transport properties of the carriers (velocity overshoot), especially important for submicron devices.

Therefore numerical simulations are necessary which solve both the continuity and the POISSON equation. Two-dimensional solutions have been obtained for $N_{\rm m} \leq 10^{17} {\rm cm}^{-3}$ only, because of the very high demands on memory capacity and computing time with increasing N_D (see e.g. /17/). Recently a one-dimensional model was proposed which properly takes into account the two-dimensional electric field distribution along the channel and the current displacement into the substrate /20/. It also includes nonstationary electron dynamics. This model was adapted for the problems to be treated here /12/. I-V-characteristics, small-signal parameters and the shift of the threshold voltage: (2) $\Delta V_{T} = V_{T} - V_{Tnom}$

were calculated for various values N_D and L. For low doping considerable shifts appear even at L=1µm which strongly increase with shorter gate lengths (Fig.1a,b). The shift cannot be neglected neither for enhancement-type FET's ($V_{Thom} \approx -0.01V$) nor for



Fig.1: Variation of the threshold voltage V_{T} with gate length for various channel thickness ("nominal", threshold voltages) for a): $N_{D}=10^{\circ}$ cm⁻³; b) $N_{D}=10^{\circ}$ cm⁻³ exp. data: $\bullet = /1/(V_{ThOM} \approx 0V)$ $\blacktriangle = \text{this work}(V_{ThOM} \approx 1.2V)$ depletion- type FET's (V $_{\rm Tnom} \approx$ -1V). At high $\rm N_{D}$ the shift is neglectable for E-type MESFETs and less than 10% for D-type MESFETs with L $\geq 0.25 \mu m$. Since the E-type FET is especially sensitive to V_{T} -variations the elimination of short-channel effects is a major achievement. A small shift ΔV_m is synonymous with a good saturation of the DC characteristics and a low output conductance. The transconductance ${\tt g}_{\tt m}$ increases with increasing $N_{\rm D}$, too, the effect being more pronounced at shorter gate lengths, Fig.2a /7/, due to the growing influence of the velocity overshoot.



a)

b)



At very low N_{D} the absolute value of the overshoot velocity is higher than in highly doped material but for FET-operation the product of velocity and carrier concentration is important. So the increase of ${\rm g}_{\rm m}$ with higher ${\rm N}_{\rm D}$ is due to the fact that the degradation in the velocity overshoot is overcompensated by the increased number of car-

riers. Experimental results support this prediction /7/. The cut-off frequency $f_{\rm C}$ for L=1µm is not influenced by N_{D} as expected, but for L <1µm a remarkable increase to values close to 100GHz is observed, Fig.2b. Figure 2 further demonstrates that for L<0.5 μ m an optimum value N_D exists which is higher than those used todate. The simulations were performed for FET structures with uniform layer thickness. The recessed-gate structure can be included, but deep ion implantations outside the gate region cannot be simulated. It is expected that the modification of the potential distribution in the substrate - as introduced by the deeply implanted regions considerably deteriorates the FET performance already for even larger gate lengths /21/. This is not the case for the recessed structure.



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5. Experimental Results

The DC characteristics of two MESFET's with $N_{p}=1.3\cdot10^{18}$ cm⁻³, L=1.4 μ m and 0.4 μ m, made simultaneously on the same chip are shown in Fig.3a,b. The drift $\Delta V^{}_{T}$ is negligible ($\approx 2\%)\,.$ The experimental value of $\Delta V^{}_{T\!\!T}$ is even smaller than the calculated value (cf. Fig.1b). In Fig.3c the characteristics of a FET with $N_D^{\,\approx\,2.5\cdot10^{\bar17} cm^{-3}},$ L=0.5µm, is given for comparison /22/. The insufficient saturation and the more pronounced shift $\Delta V_{\rm m}$ are clearly perceptibel. Since this device is made using deep contact implantation $\Delta V^{}_{T\!\!T}$ is even larger than calculated. It was shown recently that a more shallow contact implantation reduces ΔV_{T} /21,23/. This demonstrates that a uniform layer thickness (as used in these simulations) is more advantageous. Some experimental results on transconductance and cut-off frequency are included in Fig.2a,b /7,24/. For high N_D extrinsic transconductances of 260mS/mm with L=1.2µm and $L_{SD} = 4-5\mu m$ could be achieved. The breakdown voltages are at least $V_{BGD}^{=6V}$. Our calculations are also in excellent agreement with results recently published by Onodera et al /7/ who used $N_{\rm p}=5-6\cdot10^{17} {\rm cm}^{-3}$.

6. Discussion and Conclusion

Numerical simulations and experiments demonstrate that strong short channel effects - especially a threshold voltage shift - appear if the gate length is reduced into the submicron range while the dopant concentration is held constant at values presently used $(1 \div 2 \cdot 10^{17} \text{ cm}^{-3})$. Therefore it is necessary to increase and optimize the dopant concentration (e.g. $N_D \approx 7 \cdot 10^{17} \text{cm}^{-3}$ for L×0.25µm). Simultaneously both transconductance and frequency limits increase.

Experiments have shown that the theoretical expectations are met for dopant concentrations up to $1.3 \cdot 10^{18} \text{cm}^{-3}$. The shift ΔV_{T} is even smaller than predicted. The extrinsic transconductances of 260mS/mm at L=1.2µm, L_{SD}=4µm,

 $N_{D}=1.3\cdot10^{18}$ cm⁻³ are very high. An increase of the channel doping above values presently used $(1 \div 2 \cdot 10^{17} \text{ cm}^{-3})$ leads to overall improvements in the FET performance, making an additional deep ion implantation outside the gate region less necessary and leading to an easier and more correct design of the FET and of IC's containing FET's.

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