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Refractory WN Gate Self-Aligned GaAs MESFET Technology and Its Application to Gate Array IC's

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The electrical properties of reactively sputtered WN contacts on n-type GaAs have been investigated. The large barrier height (0.84V) and the low resistivity (70μohm-cm) were obtained at 6% N_2 content in a mixed gas. Typical transconductance was 150mS/mm for 1.5-μm WN self-aligned gate GaAs MESFET. A 1k-gate GaAs DCFL gate array has been successfully fabricated by a WN self-aligned gate technology. Propagation delay times under unloaded and loaded conditions (fan-out=3, interconnection length=2mm) were 49ps/gate and 200ps/gate at 0.39mW/gate power dissipation, respectively.

(1) Introduction

The gallium arsenide (GaAs) logic is likely to prove extremely useful in high speed LSI circuits. Especially, the DCFL (Direct Coupled FET Logic) is suitable for this purpose because of its design simplicity and low power dissipation. Recently, self-aligned gate GaAs MESFET technology [1,2] has been developed using refractory metal as a gate electrode to realize higher speed DCFL ICs. A critical aspect of this technology is the selection of a refractory metal; the Schottky contact must be stable at the n^+-annealing temperature (typically 800°C).

This paper reports, in the first place, that tungsten nitride (WN) film deposited by reactive sputtering is very promising for refractory gate electrode, because of larger barrier height and lower resistivity than those of other refractory metals (WSi, TiW). Next, fabrication of self-aligned WN gate GaAs MESFET will be shown. Finally, fabrication of DCFL GaAs 1k-gate gate array will be described to demonstrate successful application of self-aligned WN gate GaAs MESFET to GaAs ICs.

(2) Metallization and properties of WN film

(a) Metallization

Metallization for WN films was carried out as follows. Several WN films were deposited with rf reactive sputtering in different mixtures of N_2 and Ar. The total sputtering pressure was kept constant at 6×10^{-3} Torr and the N_2-Ar ratio was varied by changing the partial pressure of N_2 and Ar. Wafer temperature during sputtering was below 100°C. The input rf power was constant, 200W, when the deposition rate for the WN films was approximately 50Å/min.

Peeling in the shape of sinusoidal buckling wave occured in the 1000Å thick W film. The adhesion of films sputtered onto GaAs substrate is markedly improved by adding even very small amount of N_2. Peeling was absent even after annealing of 2000Å thick WN film for 15 minutes at up to 850°C.

(b) Electrical properties

Electrical resistivity measurement was carried out for WN films deposited on a semi-insulating GaAs wafer. The four-point probe method was used. The results are shown in Fig.1 as a function of N_2 content in the sputtering gas. The open circles and the closed circles show the electrical resistivity for WN films of as-

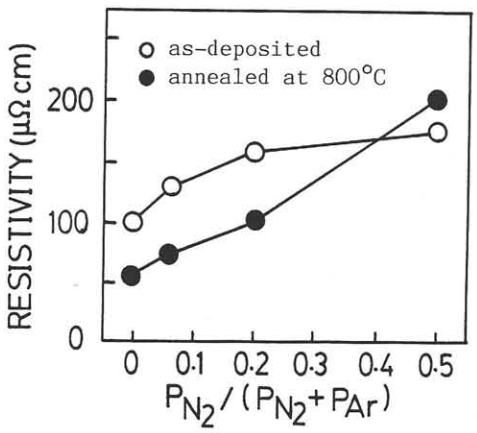

Fig.1 WN film resistivity dependence on N_2 content in N_2-Ar mixed gas.

deposited and annealed at 800°C for 15 minutes with PSG coating, respectively. The resistivity increases with partial pressure of N_2, and the resistivity is about 70 μohm-cm at 6% N_2 content in a mixed gas. The X-ray analysis revealed that the gradual resistivity increase is due to W_2N increase in the film.

Schottky contact characteristics for WN-GaAs were also evaluated by preparing WN-GaAs Schottky diodes on Si-doped n-GaAs ($n=2\times10^{15}$ cm^{-3}) layer deposited on a boat-grown n^+-GaAs substrate (Si-doped : $n=10^{18}$ cm^{-3}) by MOCVD growth. The thickness of the WN film was 1000Å and the diameter of the Schottky contact was 420μm.

The barrier height (ϕ_B) and the ideality factor (n) for the WN-GaAs Schottky diode were estimated using measured forward-biased I-V curves. This estimation was based on the following thermionic emission model, $\phi_B=(kT/q)\ln(A^*T^2/I_s)$ and $n=(q/kT)(\partial V/\partial \ln I)$, where A^* is the effective Richardson constant (here 8.4 A/cm^2K^2) and I_s is the zero voltage intercept on log(I)-V graph. Figure 2 shows the WN-GaAs Schottky contact characteristics when annealed at 800°C and 400°C for 15 minutes as a function of the N_2 content, 6%, 20%, 50%, in sputtering atmosphere. The barrier height for a WN-GaAs diode annealed at 800°C exceeds 0.8 V and slightly depends on the N_2 partial pressure. It was found that the WN film deposited at N_2=6% content atmosphere exhibited the maximum value of 0.84 V in barrier height and the minimum value of 1.16 in ideality factor. Figure 3 shows the barrier height and the ideality factor for the WN-GaAs Schottky contacts deposited at N_2=6% content in a mixed gas as a function of the annealing temperature. It should be noted that the barrier height for the WN-GaAs Schottky contact reaches the maximum at 800°C annealing temperature.

(c) Etchability

The etchability of the WN films for pattern formation is one of the most important factor when applying WN film to GaAs IC fabrication process. The selective and anisotropic fine-pattern formation of the WN film on GaAs wafer can be achieved by reactive ion etching (RIE). Figure 4 shows the etching rates for the WN film (N_2=6%) and GaAs substrate as a function of the O_2 content in a CF_4-O_2 mixed gas. The etching rate of the WN film and the etching selectivity with the GaAs substrate show maximum when the O_2 content in a mixed gas was 50%.

(3) WN gate self-aligned GaAs MESFET IC technology

The fabrication of WN gate self-aligned GaAs MESFET was carried out on commercially available undoped 2"φ LEC GaAs wafer. An n-type channel layer for normally-off FET (E-FET) was formed by $^{28}Si^+$ selective ion implantation with a dose of $1.75\times10^{12}cm^{-2}$ at 50keV, and successive capless annealing in AsH_3+Ar mixed atmosphere at 850°C for 15 minutes. The WN gates with 1500Å thick were formed using the reactive sputtering and etching technique described in previous section.

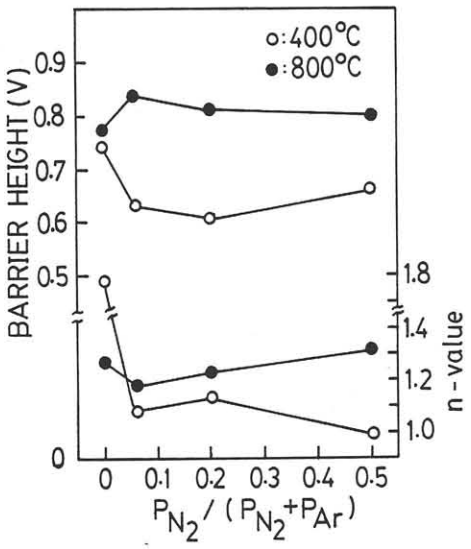

Fig.2 Schottky barrier height and ideality factor of WN on GaAs as a function of N_2 content in N_2-Ar mixed gas.

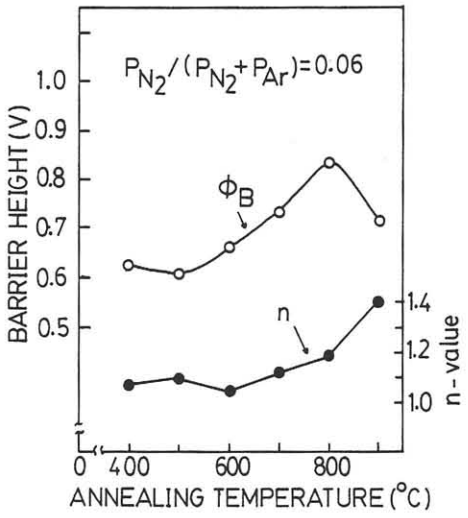

Fig.3 Schottky barrier height and ideality factor of WN on GaAs as a function of annealing temperature.

The source and drain n^+-regions were formed by Si^+ implantation which was self-aligned to the gate electrode with a dose of 3.0 x $10^{13}cm^{-2}$ at 180keV, followed by the annealing at 800°C for 10 minutes with a PSG encapsulating film to activate dopants. The ohmic contacts were made with AuGe/Au alloy. Figure 5 shows the typical I-V characteristic of a self-aligned E-FET with 1.5μm long and 20μm wide gate. Typical transconductance g_m was about 150 mS/mm.

In order to evaluate the switching performance of a self-aligned FET, E/D type DCFL 15-stage ring oscillators were fabricated using planar process technology. The gate for the normally-on FET (D-FET) was 1.5μm long and 10μm wide. Si^+ implantation was made at 50 keV with a dose of 3.5 x $10^{12}cm^{-2}$ for D-FET. The n^+-regions were formed by the same process as previously mentioned. The interconnection metallization was made by Ti/Pt/Au for the first and second levels. The insulating film between the first and second interconnection was 6000Å thick CVD SiO_2. The average values of the threshold voltage (V_T) across a wafer were +0.05 V for E-FET and -0.40V for D-FET. The minimum propagation delay time (t_{pd0}) was 49 ps/gate for the power dissipation of 0.39 mW/gate at V_{DD}=1.0 V.

(4) 1k-gate gate array and its application to 4-bit Arithmetic and Logic Unit (ALU)

A 1k-gate gate array with DCFL circuit, shown in Fig.6, was successfully fabricated using WN gate self-aligned GaAs MESFET technology. This gate array includes several kinds of ring oscillator circuits and a 4-bit ALU circuit. The chip size is 3.75mm x 3.75mm, in which 1050 gates are integrated. Detailed descriptions for this 1k-gate gate array were previously reported.[3)]

Table 1 summarizes the unloaded propagation delay time (t_{pd0}) and the propagation delay time increments by interconnection line length (Δt_{pd}/mm), fan-out (Δt_{pd}/FO) and crossover (Δt_{pd}/co). Propagation delay time (t_{pd}) under typical loading condition in an actual IC can be estimated using these results. If 2 mm interconnection length and 3 fan-outs are taken as average loading conditions, the propagation delay time becomes 200ps/gate at 0.39 mW/gate power dissipation, whereas the propagation delay time of 284 ps/gate at 0.2 mW/gate power level under the same loading condition was obtained using Pt buried gate technology.[3)]

High speed testing for the 4-bit ALU was performed at V_{DD}=1.5 V for the chip which passed the low frequency test by using a probe card modified and calibrated for a 50 ohm testing

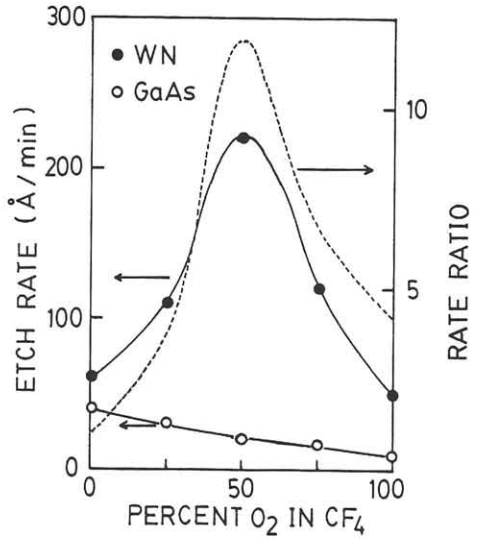

Fig.4 WN and GaAs etching rates and etching selectivity as a function of the O_2 content in CF_4-O_2 mixed gas.

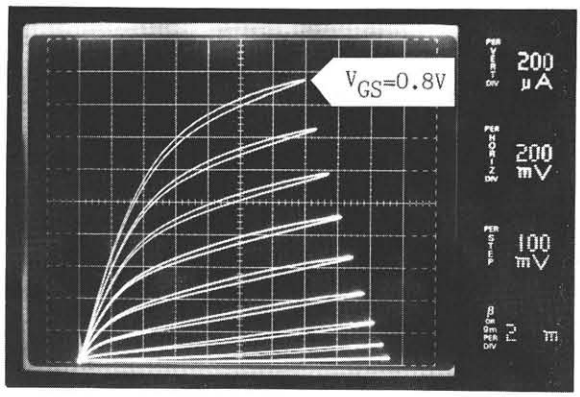

Fig.5 Typical I_D-V_D curve of WN self-aligned gate GaAs MESFET with L_g/W_g=1.5μm/20μm.

Table 1 Fundamental performance of GaAs 1k-gate gate array.

(Pd=0.39mW, V_{DD}=1V)

t_{pd0}	Δt_{pd}/mm	Δt_{pd}/FO	Δt_{pf}/co
49ps	50ps	23ps	0.9ps

system. Figure 7 shows the switching waveforms of the ALU displayed on an oscilloscope. The 3.5 ns carry signal delay time was measured for the add function by applying 1111 and S000 to the data inputs, where S went from 0 to 1 state. The total power dissipation in a chip was 122mW. This result shows high speed and low power performance of the circuit.

(5) Summary

The electrical properties of reactively sputtered WN film contacts on n-type GaAs have been investigated; (1) Dependence of the resistivity of WN film on N_2 content in the N_2-Ar mixed gas, (2) Dependence of WN-GaAs Schottky contact characteristics on N_2 content and annealing temperature. The maximum barrier height (0.84V) and the low resistivity (70μohm-cm) were obtained at 6% N_2 content in a mixed gas. It is applicable to self-aligned refractory gate metal, because of its high temperature stability, large barrier height and good adhesion. WN gate self-aligned GaAs MESFET has been fabricated. Typical transconductance was 150mS/mm for 1.5μm gate FET. A 1k-gate GaAs DCFL gate array including ring oscillators and a 4-bit ALU circuit has been successfully fabricated by a WN self-aligned gate technology. Mimimum propagation delay times were 49ps/gate and 200ps/gate at 0.39mW/gate power dissipation for the unloaded and loaded circuits, respectively. Calculation time of ALU circuit was measured to be 3.5ns. These preliminary experimental data suggest that WN self-aligned gate GaAs MESFET technology is well suited for fabricating high speed GaAs LSIs.

Acknowledgement

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References

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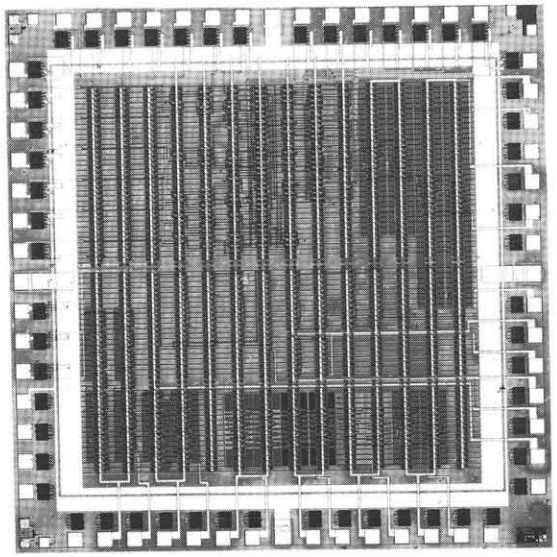

Fig.6 Photomicrograph of 1k-gate gate array including 4-bit ALU circuit.

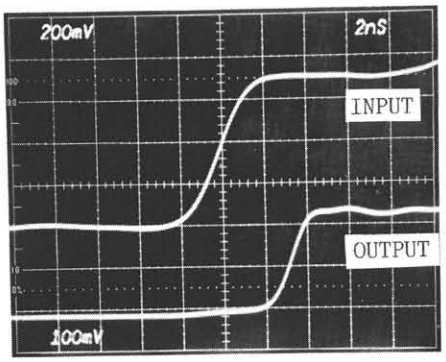

Fig.7 Input and output waveforms for 1111+S000 arithmetic add function of ALU circuit. Carry signal output was picked up when input S went from 0 to 1 state.