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A Large Logic Swing and High Speed DCFL with GaAs MASFET's

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A GaAs MASFET (Metallic Amorphous Silicon gate FET) demonstrates a large logic swing and high speed in DCFL because a MASFET gate electrode is formed with a large barrier height Schottky contact between a-Si-Ge-B (amorphous- silicon- germanium-boron) and n-GaAs. A DCFL inverter with a GaAs MASFET exhibits a clamp level as high as 0.94 V. A ring oscillator with GaAs MASFETs shows minimum propagation delay time of 16.4 ps. MASFETs have feasibility to increase GaAs LSI's fabrication yield considerably.

1. INTRODUCTION

GaAs LSIs are usually composed of MESFETs in DCFL configuration, because GaAs does not have adequate oxide or insulator film to form MOS or MIS devices. In addition, DCFL is suitable for GaAs LSIs because of the circuit simplicity, high speed and low power operation. However, DCFL logic swing with GaAs MESFETs is small because its high level is restricted to the barrier height (about 0.7 V) of the metal/GaAs Schottky gate contacts due to gate current injection. Consequently, threshold voltage dispersion must be less than 25 mV to satisfy GaAs LSI's operation margin. However, the threshold dispersion of GaAs MESFET (for example, GaAs SAINT FET[1]) is larger than 50 mV[2]. The development of GaAs LSIs composed of more than 10,000 FETs is difficult with this dispersion. One way to overcome this difficulty is to enlarge the barrier height of the gate contact.

A large logic swing GaAs DCFL was developed using new structure FETs, GaAs MASFETs (Metallic Amorphous Silicon gate FETs). In the new device, a-Si-Ge-B/n-GaAs contact is utilized to the gate electrode. A contact between a-Si-Ge-B[3,4,5] and GaAs forms a Schottky barrier of a height as large as 0.90-0.98 V[6,7,8]. A large barrier height of gate enlarges DCFL circuit logic swing. Thus a GaAs MASFET has the potential for realizing full-bit operation of GaAs LSIs even with an FET threshold voltage dispersion of 40-50 mV.

In addition, high speed operation can be expected for DCFL with GaAs MASFET because the FET maximum drain saturation current $I_{ds}(MAX)$ is large due to the large built-in gate voltage, V_{bi}, roughly estimated as $I_{ds}(MAX)=KV_{bi}^{2}$ (K; a coeffitient).

This paper presents the characteristics of a-Si-Ge-B/n-GaAs contact with 1 V barrier height, normally-off GaAs MASFET characteristics with a large transconductance and a large drain saturation current, a E/R type inverter of a high output voltage, and 25-stage ring oscillators to demonstrate the high switching speed of DCFL circuits with MASFETs.

2. A LARGE BARRIER HEIGHT CONFIRMATION

An amorphous Si-Ge-B film was deposited on a GaAs wafer by thermal decomposition of a silane-germane-diborane mixture in a low pressure furnace at 450°C. Film and contact properties are controlled by adjusting flow ratios among these gases. In this experiment, flow-rate ratios of the reactant gases were

$GeH_4/(SiH_4+GeH_4)$ = 5 % and

$B_2H_6/(SiH_4+GeH_4)$ = 2 %.

The resistivity of the film fabricated under this condition was 4.4 ohm·cm.

For evaluating contact characteristics, a diode shown in Fig.1a was provided. The contact

was formed on an n-layer prepared by ion implantation at 60 KeV with 2.5×10^{12} cm^{-2} dosage into S.I.GaAs wafer. The peak carrier density of the n-layer was 2×10^{17} cm^{-3}.

The forward and backward current-voltage (I-V) characteristics of the diode are shown in Fig.1b. Barrier height is obtained from the forward I-V curve by fitting to the following equations;

$$J=J_s(\exp(qV/nkT)-1), \quad ---(1)$$

$$J_s=A^{**}T^2\exp(-q\phi_{bn}/kT). \quad ---(2)$$

Barrier height was found to be 1.00 V with n=1.14, assuming that $A^{**}=8.16$ $A/cm^2/K^2$. This is the largest barrier height among the values obtained for a-Si-Ge-B/GaAs systems[7].

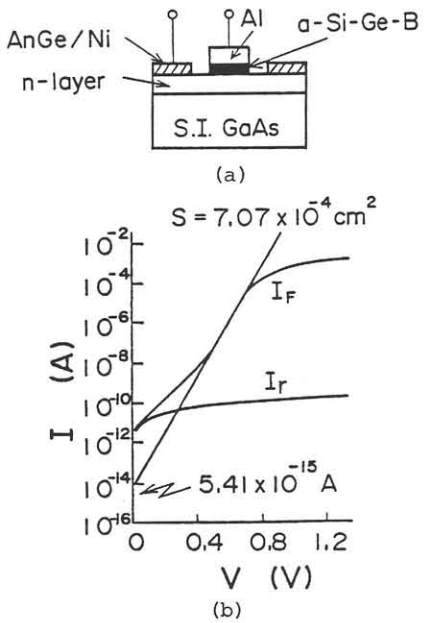

Fig.1 (a) An a-Si-Ge-B/n-GaAs diode structure.
(b) Forward I-V characteristics of the diode.

3. HIGH TRANSCONDUCTANCE GaAs MASFET

A GaAs MASFET structure is shown in Fig.2. The MASFET was fabricated by the SAINT process[1] where heavily doped source and drain regions were self-aligned. The gate electrode was made of Al/a-Si-Ge-B. Aluminum reduces the gate electrode resistance and also behaves as an etching mask when defining the amorphous film by CF_4+5%O_2 gas plasma. Amorphous film thickness was 1500 A. Gate resistance due to the amorphous film was estimated to be about 165 ohm for 1 μm x 40 μm gate.

The channel FET layer was formed in an S.I.GaAs wafer with 1.5×10^{12} cm^{-2} dosage Si ion implantation at 60 KeV. The n^+-layer formation was carried out with a 4×10^{13} cm^{-2} dosage Si ion implantation at 200 KeV through PCVD SiN film.

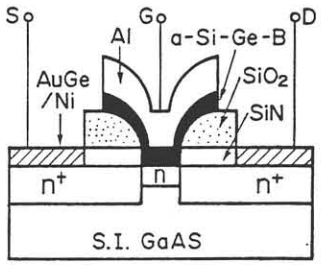

Fig.2 Cross section of a GaAs MASFET fabricated by the SAINT process.

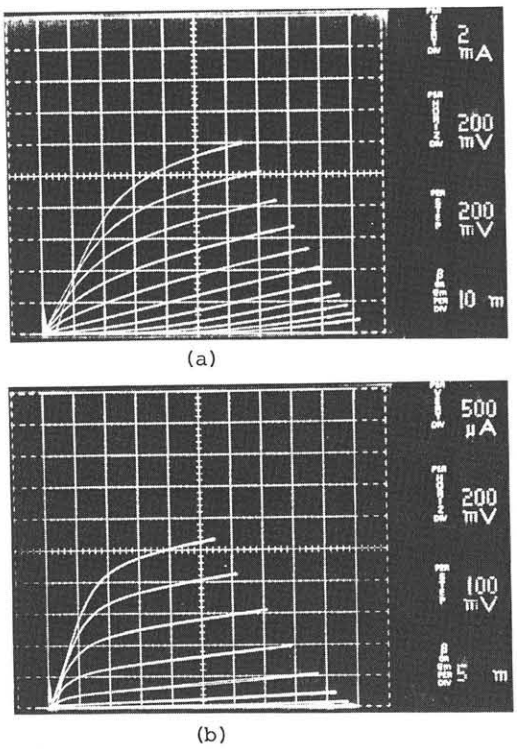

Fig.3 Characteristics of two GaAs MASFET of different gate length. Gate width is 40 μm.
(a) l_g=0.5 μm, V_{th}=-0.95 V, V_g=-0.9-1.1 V.
(b) l_g=1 μm, V_{th}=0.38 V, V_g=0-1.0 V.

The I_d-V_d characteristics of a 40 μm width and 0.5 μm length gate GaAs MASFET are shown in Fig.3a, and those of a 1 μm length gate GaAs MASFET in Fig.3b. The device parameters derived from the I_d-V_d characteristics are summarized in Table 1. The FETs shown in Fig.3 are monitor devices for an inverter and ring oscillators described later.

The key feature in Table 1 is that the 1 μm gate MASFET exhibits transconductance g_m as large as 150 mS/mm despite the high threshold voltage of 0.38 V. This is resulted from the large barrier

Table 1 Measured parameter of MASFETs

	(a)	(b)
gate length (μm)	0.5	1.0
V_{th} (V)	-0.95	0.38
g_m (mS/mm)	250	150
K ($mA/V^2/10\mu m$)	0.86	1.80
I_{ds} ($mA/10\mu m$)	2.8	0.65

g_m and I_{ds} were measured at V_g=0.9 V and V_D=1 V.

height of the gate contact. GaAs MASFET of 0.5 μm gate length also show a large transconductance of 250 mS/mm. Although both gate length FETs were fabricated on the same wafer, threshold voltages were different. This is due to short channel effect[9].

4. LARGE LOGIC SWING REALIZATION

The large barrier height of the a-Si-Ge-B/GaAs contact increased logic swing of an E/R inverter, which was composed of a 40 μm width and 1 μm length gate driver MASFET and a load resistor. The inverter transfer characteristics are shown in Fig 4. The load resister was estimated to be 420 ohm by a monitor located near the inverter. Bias voltage, V_{DD}, varied from 0 to 1.5 V by 0.1 V step. Figure 5 shows the output voltage, V_{out}, at the input voltage of V_{in}=0 V as a function of the bias voltage, V_{DD}. It is noted from the figure that clamping of V_{out} starts at 0.94 V. On the other hand, clamping for conventional MESFETs usually starts at about 0.7 V. Therefore, the DCFL logic swing high level is improved by the barrier height increment with MASFET.

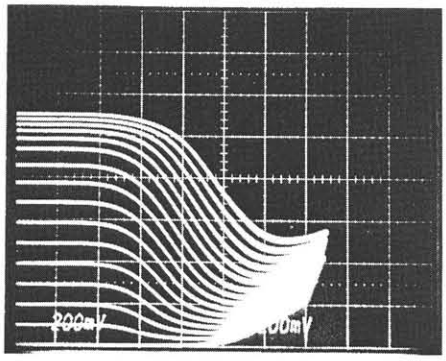

Fig.4 Transfer characteristics of an E/R inverter, where the driver FET is a 40 μm width and 1 μm length GaAs MASFET.

This improvement noticeably affects the yield of GaAs LSIs with DCFL. To confirm the improvement in LSIs, the allowable dispersion of threshold voltage and average threshold voltage ranges were estimated for a GaAs LSI with 10,000 gates. Resuls are shown in Fig.6, where triangular areas between two oblique lines are within the allowable range. For this estimation, the following assumption has been made:

(a) Threshold voltage dispersion is gaussian.

$$f(V_{th})=1/((2\pi)^{1/2}\sigma(V_{th}))\exp(-(V_{th}-\overline{V}_{th})^2/2\sigma(V_{th})^2) \quad ---(3)$$

$$\phi(V_{th})=\int_{-\infty}^{V_{th}} f(V_{th}')dV_{th} \quad ---(4)$$

(b) Low level V_L is 0.1 V.

(c) Load current I_L is 0.1 mA/10μm.

(d) K-value is 1.8 $mA/V^2/10\mu m$.

(e) V_{th} range is defined by the following restriction:

$V_{th} > V_L$, namely

$$N_{E-FET}\cdot\phi(V_{th}=0.1\ V) < 0.5 \text{ and} \quad ---(5)$$

$$I_{on}(=K(V_H-V_{th})^2) > 1.5I_L, \text{ namely}$$

$$N_{E-FET}\cdot(1-\phi(V_{th}=V_H-(1.5I_L/K)^{1/2})) < 0.5, \quad ---(6)$$

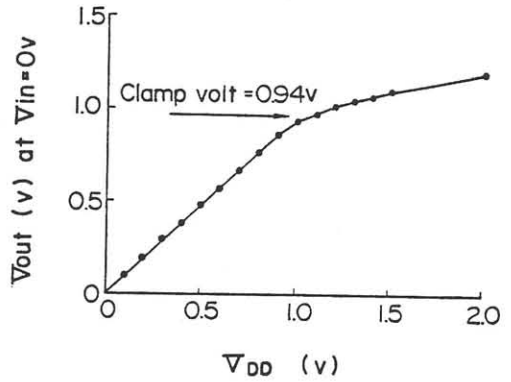

Fig.5 Relationship between bias voltage, V_{DD}, and output voltage, V_{out}, at the input voltage, V_{in},=0 V for the E/R inverter shown in Fig.4.

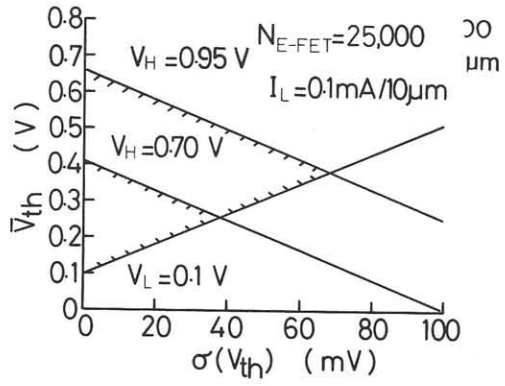

Fig.6 Estimation of allowable dispersion, $\sigma(V_{th})$, and range of average threshold voltage, $\overline{V}_{th}$.

where $\sigma(V_{th})$ is the standard deviation of threshold voltage, $N_{E\text{-}FET}$ a number of E-FET in a LSI chip (2.5 E-FETs for each gate were assumed), V_H a high level and V_L a low level. It is clearly seen that 10,000-gate LSIs can be successfully realized with a 50 mV threshold dispersion by adopting MASFET.

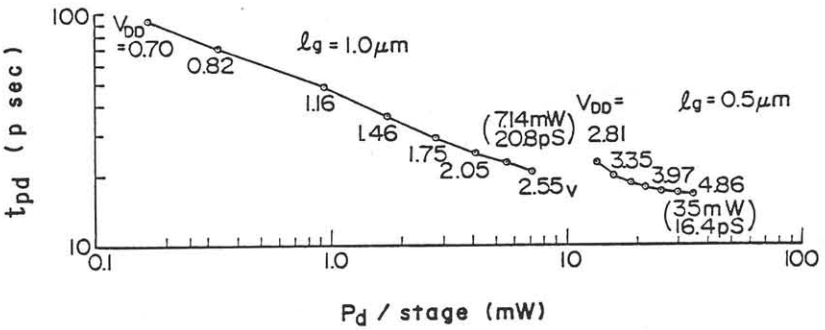

Fig.7 Propagation delay time versus power dissipation for 25-stage ring oscillator composed of GaAs MASFETs.

5. GaAs MASFET DYNAMIC PERFORMANCE

To confirm the high speed switching operation of MASFET, 25-stage ring oscillators were fabricated. Each inverter consists of a 40 μm wide driver MASFET and an n^+-layer resistor load. Figure 7 presents the propagation delay time versus the power of two ring oscillators. Each corresponds to the 0.5 μm and the 1 μm gate driver MASFET shown in Fig.4. Results show superior speed-power performance due to large I_{ds} or g_m of driver FETs. A minimum propagation delay time of 16.4 ps was obtained with the 0.5 μm gate ring oscillator. For the 1 um gate ring oscillator, minimum propagation delay time was 20.8 ps. This is the smallest value ever reported for normally-off 1 μm gate FETs.

6 SUMMARY

(1) Newly tested a-Si-Ge-B/n-GaAs diodes showed barrier height as large as 1.0 V.

(2) A normally-off GaAs MASFET of V_{th}=0.38 V showed transconductance as large as 150 mS/mm.

(3) Output voltage of a DCFL inverter with MASFET increased up to 0.94 V.

(4) High speed operation of the DCFL circuit with MASFET was confirmed by 25-stage ring oscillators. Minimum propagation delay time was 16.4 ps.

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