Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 391-394



# Experimental and Theoretical Studies on Short Channel Effects in Lamp-Annealed $WSi_x$-Gate Self-Aligned GaAs MESFET's

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In this paper, short channel effects in $WSi_x$-gate self-aligned GaAs MESFETs are studied, using the lamp annealing method as well as the furnace annealing method, and device simulation, including lateral spread and diffusion of $n^+$-dopant. It was found that lateral diffusion of $n^+$-dopant in $WSi_x$-gate self-aligned GaAs MESFETs, fabricated using the furnace annealing method, significantly affects device parameters and causes short channel effects at gate lengths less than 1.5 $\mu$m. However, the lamp annealing method was found to be effective to reduce the short channel effects, even at a gate length of 0.6 $\mu$m, due to minimizing the lateral diffusion.

## 1. Introduction

In recent years, GaAs LSIs with more than 10,000 gates have been successfully fabricated, using self-aligned technology, with gate lengths of 1.0 or 1.5 $\mu$m [1],[2]. However, swiching performance was not sufficient to surpass high-speed Si LSIs. In order to further improve the swiching performance of GaAs LSIs, the gate length of FETs must be reduced to less than 1.0 $\mu$m. As the gate length is reduced, however, short channel effects become the most crucial factors to prevent further performance improvement. These short channel effects include 1) threshold voltage shift to the negative side[3], 2) dependence of threshold voltage on source-drain voltage, 3) poor current cutoff in the subthreshold region[4], and 4) reduction in K-value[5]. Due to these effects, the controllability and the reproducibility of device parameters have also been insufficient. Therefore, understanding and controlling these effects is indispensable to realizing very high-speed GaAs LSIs.

The principal purpose of this paper is to clear up the cause of short channel effects in $WSi_x$-gate self-aligned GaAs MESFETs[6] by investigating, theoretically as well as experimentally, how the lateral stretch of $n^+$-dopant affects device parameters. For this purpose, gate-length dependence of device parameters in lamp-annealed FETs (L.A.FETs) is characterized and compared with that in conventional furnaced annealed FETs (F.A.FETs). From these, lateral stretch, including lateral spread (during implantation) and lateral diffusion (during annealing) are estimated using a one dimentional device simulation.

## 2. Experimentals and results

Self-aligned FETs, having different 8 gate lengths, were fabricated on [100] semi-insulating GaAs substrates through various post $n^+$-implantation annealing prcedure. The gate width was 30 $\mu$m. $Si^+$-implantation for n- and $n^+$-layer was performed at 59 KeV with a dose of $1.0 \times 10^{12}$ $cm^{-2}$, and at 175 KeV with a dose of $1.7 \times 10^{13}$, respectively. A 12 sec lamp annealing at 1,000 °C and a 900 sec furnace annealing at 850 °C were carried out for n-layer formation for L.A.FETs and F.A.FETs, respectively. It was confirmed, from electrical and metallurgical characteristics that $WSi_x$/n-GaAs Schottky contacts were not subjected to interfacial degradation during these annealing processes[8].

A well known short channel effect is threshold voltage shift to the negative side as gate length is decreased [3],[4],[5],[7]. Fig. 1 shows the threshold voltage, $V_{th}$, measured as a function of gate length for both L.A.FETs and F.A.FETs. The annealing conditions for the $n^+$-layer for L.A.FETs and F.A.FETs were 960 °C and 5 sec, and 750 °C and 900 sec, respectively. As is clear from this

figure, the threshold voltage of F.A.FETs shifts remarkably to the negative side for gate lengths less than 1.5 μm. At a 0.7 μm gate length, the drain current of the FETs was not pinched off, exhibiting extremely high drain conductance. On the other hand, in L.A.FETs, the shift is comparatively small even at a 0.6 μm gate length.

Another aspect of short channel effects is that threshold voltage depends strongly on source-drain voltage, $V_{ds}$, with reduced gate length. Here, we express this phenomenon using following relation,

$$V_{th} = V_{tho} + \gamma V_{ds}, \qquad (1)$$

where $\gamma$ is a parameter indicating the degree of the effect. Fig. 2 shows the parameter, $\gamma$, in L.A. and F.A.FETs, as a function of gate length. In F.A.FETs, $\gamma$ increases rapidly for gate lengths less than 1.5 μm, while in L.A.FETs $\gamma$ is comparatively constant down to a gate length of 0.6 μm.

The magnitude of the subthreshold current, $I_{sub}$, is also one criterion of the short channel effects. The subthreshold current is known to be proportional to the factor $\exp(qV_g/n_gkT)$ in the subthreshold region, where q is electron charge, $V_g$ gate bias voltage, k Boltzmann's constant, T temperature, and $n_g$ a parameter exhibiting the degree of subthreshold-current cutoff[4]. Fig. 3 shows the parameter $n_g$ in L.A. and F.A.FETs as a function of the gate length. Note that $n_g$ in L.A.FETs is comparatively constant even in the gate length-range from 0.6 to 1.0 μm, while in F.A.FETs, $n_g$ increases rapidly in the gate lengths less than 1.5 μm.

Fig. 4 shows K-value in L.A. and F.A.FETs as a function of the gate length, where K is a factor in FET performance expressed as follows,

$$K = \varepsilon\mu W_g/2dL_g, \qquad (2)$$

where $\varepsilon$ is the dielectric constant, $\mu$ the drift mobility of electrons in the n-layer, d the effective thickness of the n-layer, $W_g$ gate width, and $L_g$ gate length. Note that K-value for F.A.FETs exhibits an anomalous decrease at a gate length of 1.3 μm. However, such a decrease is not observed for L.A.FETs.

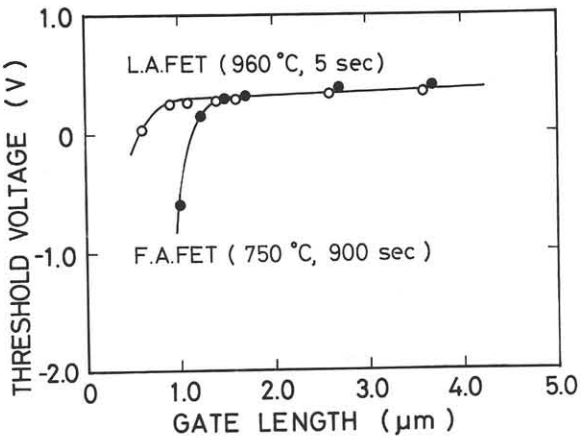


Fig. 1 Gate-length dependence of threshold voltage in L.A. and F.A.FETs.

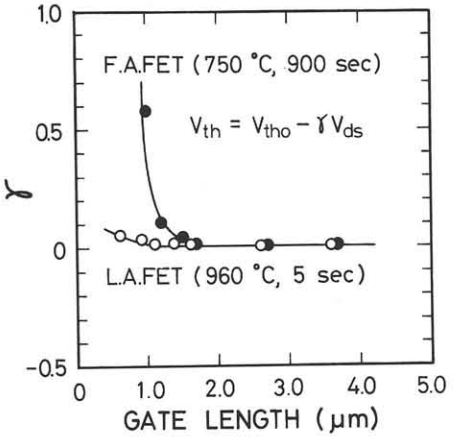


Fig. 2 Gate-length dependence of parameter, $\gamma$, in L.A. and F.A.FETs. $\gamma$ indicates the magnitude of the dependence of threshold voltage on source-drain voltage.

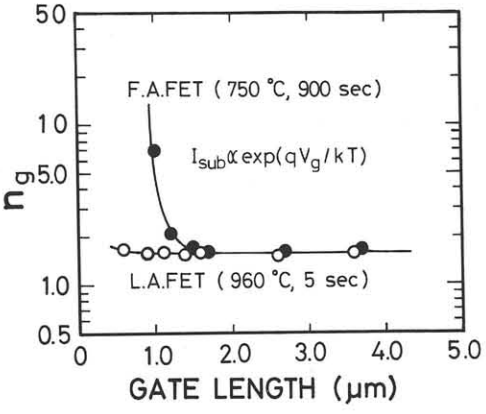


Fig. 3 Gate-length dependence of parameter, $n_g$, in L.A. and L.A.FETs. $n_g$ indicates the degree of subthreshold-current cutoff.

3. Discussion

Short channel effects are considered to be due to lateral stretch of $n^+$-dopant, including lateral spread (during implantation) and lateral diffusion (during annealing) [7],[4],[5]. In order to estimate lateral stretch, we carried out a theoretical study, using a one dimentional device simulation. In this simulation, LSS theory was employed for the vertical and lateral carrier profile, including the effect of lateral diffusion in a factor of lateral strech, $L^+_{//}(t, T)$, as

$$L^+_{//}(t, T) = \sqrt{\Delta R^{+2}_{//} + 2D^+_{//}(T)t}, \qquad (4)$$

where $\Delta R^+_{//}$ and $D(T)^+_{//}$ are lateral spread and lateral diffusion coefficients of $n^+$-dopant, respectively. Here, $\sqrt{2D^+_{//}(T)t}$ indicates diffusion length, $X^+_{//}(t, T)$, at an annealing temperature, T, for an annealing time, t. Fig. 5 shows the gate-length dependence of threshold voltage in L.A.FETs annealed at 760 °C for 480 sec, as an example. Open circles indicate experimental results, and solid and broken lines simulated results. From this figure, it appears that the solid line is the most appropriate one, and consequently, $L^+_{//}(480, 760)$ was estimated to be 263 nm. The same procedure was applied to the other lamp-annealed samples under different conditions. The open circles in Fig. 6 show lateral stretch as a function of the square root of annealing time. It is clear from Fig. 6 that a linear relationship is established between square root of annealing time and lateral stretch. $\Delta R^+_{//}$ can be obtained from the extrapolated lateral stretch at an annealing time of 0 sec. $D^+_{//}(t, T)$ can be obtained from the slope of the extrapolated line. $\Delta R^+_{//}$ obtained here, 100 nm, is nearly equal to that obtained by LSS theory, 984 nm. Fig. 7 shows an Arrhenius plot of the diffusion coefficient, $D^+_{//}(t, T)$, obtained from Fig. 6. From this figure, we can estimate the activation energy, $E^+_{a//}$, and the frequency factor, $D^+_{0//}$, for a lateral diffusion of $n^+$-dopant to be 1.2 eV and $2.2 \times 10^{-6}$ $cm^2/sec$, respectively.

It was also confirmed that sheet resistivity of the $n^+$-layer, $\rho_s$, reaches a saturation value, $\rho_s = 120\,\Omega/\square$, after lamp annealing at 950 °C for 5 sec or less. In furnace annealing, more than 900 sec of annealing time was required to decrease

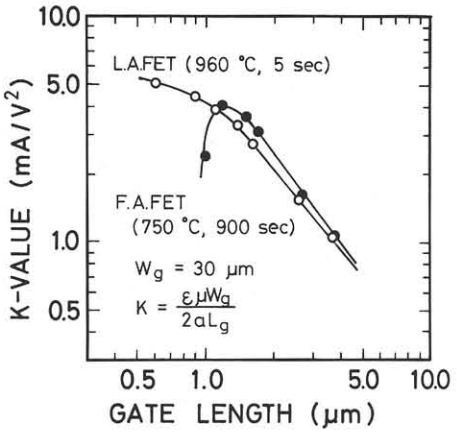


Fig. 4 Gate-length dependence of K-value in L.A. and F.A.FETs.

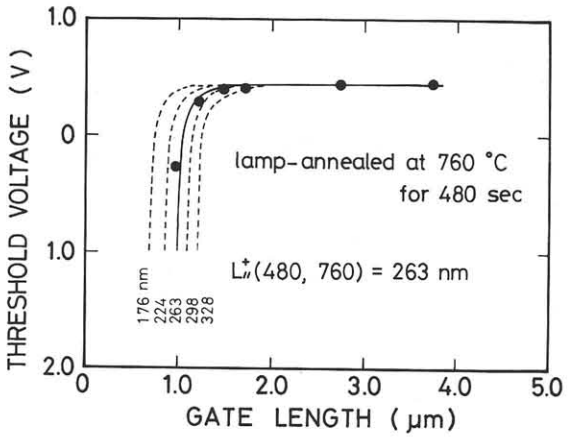


Fig. 5 Gate-length dependence of threshold voltage for L.A.FETs annealed at 760 °C for 480 sec. Open circles indicate experimental results, and solid and broken lines, theoretical results. The solid line is the most appropriate.

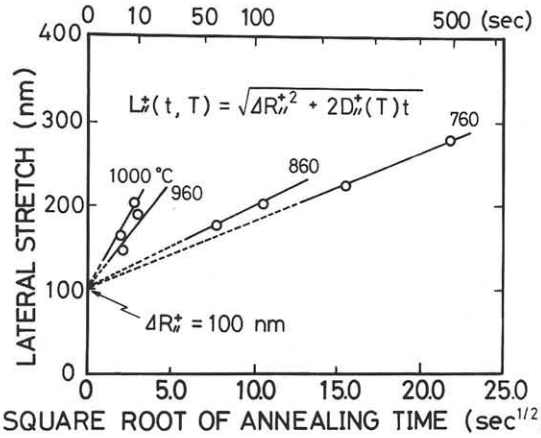


Fig. 6 Annealing-time dependence of lateral strech as a parameter of annealing temperature.

the sheet resistivity to a saturation value of about 200 Ω/□ at 750 °C. Therefore, when we carried out 900 sec furnace annealing at 750 °C, lateral diffusion length, $X^{+}_{//}(900, 750)$, and the lateral strech, $L^{+}_{//}(900, 750)$, can be estimated to be 222 nm and 243 nm, respectively. Under a lamp annealing conditions of 950 °C, 5 sec, $X^{+}_{//}(5, 950)$ and $L^{+}_{//}(5, 950)$ are estimated to be 50 nm and 111 nm, respectively. Notice that $X^{+}_{//}(5, 950)$ is less than one fourth of $X^{+}_{//}(900, 750)$, and consequently, $L^{+}_{//}(5, 950)$ is less than a half of $L^{+}_{//}(900, 750)$.

Lateral stretch primarily causes reduction of the effective gate length, and should result in improvement in FET performance. In fact, K-value in F.A.FETs is larger than that in L.A.FETs at the gate lengths of more than 1.3 μm, due to the comparatively large diffusion length. However, the K-value is decreased as lateral stretch becomes comparable with gate length, because the $n^{+}$-layer for the source region overlaps that for the drain region under the gate electrode, resulting in an increase of carrier concentration and the effective thickness of the n-layer. Of course, then, the threshold voltage shifts to the negative side. It is found that using the lamp annealing method, the $n^{+}$-layer can be sufficiently activated by suppressing lateral diffusion, resulting in a reduction of short channel effects, and consequently, an improvement in FET performance.

## 4. Summary

After experimental and theoretical studies of the gate-length dependence of FET parameters, it was confirmed that the lateral spread and lateral diffusion of $n^{+}$-dopant adversely affect the performance of $WSi_x$-gate self-aligned GaAs MESFETs having gate lengths of 1.5 μm or less. It was also found that the lamp annealing method is effective to reduce the short channel effects because the lateral diffusion of the $n^{+}$-dopant can be suppressed with a short annealing cycle, resulting in an improvement of FET performance even at submicron gate length around 0.6 μm.

The authors wish to express their thanks to T. Misugi, M. Kobayashi, M. Fukuta, and A. Shibatomi for their continuing encouragement, to Y. Nakayama, T. Inada for valuable discussions, and to S. Suzuki for his assistance in fabrication.

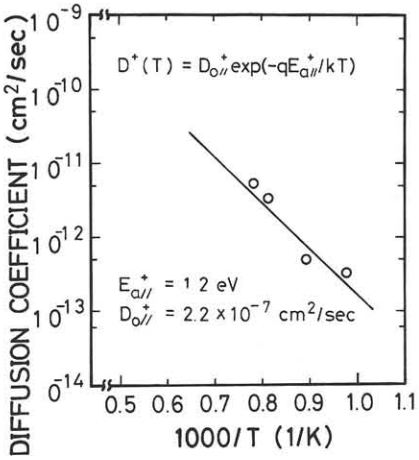


Fig. 7 Arrhenius plot of diffusion coefficient of $n^{+}$-dopant.

## References

[1] Yokoyama et al., ISSCC Digest of Technical Papers, p 44, Feb. 1984.

[2] M. Hirayama et al., ISSCC Digest of Technical Papers, p 46, Feb. 1984.

[3] C. P. Lee et al., Appl. Phys. Lett. 37(3), pp. 311-313.

[4] N. Kato et al., IEEE Electron Device Lett., EDL-4 417 (1983).

[5] N. Yokoyama, et al., Appl. Phys. Lett. 42 , 270 (1983).

[6] Yokoyama, et al., ISSCC Digest of Technical Papers, p. 44, 1983.

[7] K. Matsumoto, et al., Int. Symp. GaAs and Related Compound, 1982, p. 317.

[8] T. Ohnishi et al., IEEE Electron Device Lett., to be published.