Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp. 399-402

Super-Buffer FET Logic (SBFL): A Logic Gate Suitable to GaAs LSI's

Koutarou Tanaka, Hiroshi Nakamura, Yasushi Kawakami, Masahiro Akiyama,
Toshimasa Ishida, and Katsuzo Kaminishi

Research Laboratory, OKI Electric Industry Co., Ltd.
550-5, Higashiasakawa-cho, Hachioji, Tokyo 193, Japan

For GaAs LSIs, we propose one unit logic gate with low power consumption. This logic gate is named SBFL (Super-Buffer FET Logic), which is constracted by super-buffer circuit. SBFL has large advantages of lower output low-level, larger noise margins and higher load drivability. This paper shows these nature of SBFL compared with DCFL through the measurement and the simulations.

I. Introduction

Recent advances in GaAs MESFET fabrication technology [1)-3)] have enabled the reproducible fabrication of normally-off MESFET (enhancement-type FET: E-FET) with high g_m and small V_{th} scattering. Therefore, the large scale integrated circuits have been able to be fabricated by using a direct coupled FET logic (DCFL) circuit [4),5)]. The DCFL circuit has large advantages of simplicity, low power consumption and the need of only one supplied voltage. Certainly, the unloaded propagation delay time (raw speed) of DCFL is very excellent. However, as the scale of integration increases, the problem of low drivability has become more and more serious. Because the load drivability of DCFL is limited by the I_{dss} of pull-up FET, it cannot be increased without increase of power consumption.

In this paper, one unit logic gate with high load drivability and low power consumption is described. This logic gate is constructed by inverted super-buffer circuit which is well known in Si NMOS circuits. After the basic conception of this logic gate is briefly shown, the static and dynamic characteristics of this logic gate including the property of load drivability are described.

II. Unit Logic Gate

Figure 1 shows the unit circuit of the inverter along with a DCFL. Because it is constructed by super-buffer circuit, we call this logic gate super-buffer FET logic (SBFL). Usually, both of the second pull-up FET (Q_3) and pull-down FET (Q_4) are E-FET. However an FET type of the second pull-up FET (Q_4) can be chenged to normally-on FET (depletion-type FET : D-FET). When these two SBFL circuits are distinguished, we call them SBFL-E and SBFL-D, respectively. The NOR gate can be realized by connecting additional Q_3' and Q_4' parallel to Q_3 and Q_4 as shown by the broken lines.

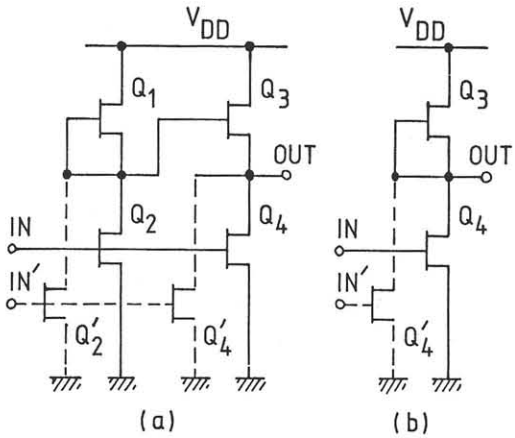

Fig. 1 The unit circuits of SBFL (a) and DCFL (b). The configuration of NOR circuits are also shown by the broken lines.

In Fig. 1, when the input signal changes from low level to high level, in addition to opening the second pull-down FET (Q_4), the second pull-up FET

(Q_3) closes after a little time. The closing of Q_3 helps Q_4 to absorb the charge from the capacitive load, and it reduces a steady-state current. When the input signal turns to low level, in addition to closing the second pull-down FET (Q_4), the second pull-up FET (Q_3) opens after a little time. Because the output of the first-stage E/D gate is connected only to the gate of the second pull-up FET (Q_3), the gate-sourse voltage of the Q_3 can be increased up to built-in voltage. While the output level is still low, the current through Q_3 to the capacitive load reaches the maximum value. This motion cannot be realized by the structure of non-inverted super-buffer circuits in Si NMOS circuits. After the output level has reached high level, the drain current of Q_3 is fairly decreased if the supplied voltage is optimized.

In this SBFL action, the load drivability is caused by the transient current flow. Therefore, high performance FET's will increase the load drivability without much increase in power dissipation. In DCFL, on the contrary, it is impossible to increase the load drivability without the increase in power dissipation.

Table I Process condition and the properties of obtained MESFET's.

		E-FET	D-FET
Gate Length	(μm)	1.0	1.0
Ion Implantation (^{29}Si)			
Active Layer			
Energy	(KeV)	60	60
Dose	(cm^{-2})	1.4×10^{12}	2.1×10^{12}
n^+ Layer			
Energy	(KeV)	100	100
Dose	(cm^{-2})	1.5×10^{13}	1.5×10^{13}
Threshold Voltage: V_{th}			
Mean Value	(mV)	+2	-509
Standard Deviation	(mV)	26	34
I_{ds} Vgs	(V)	0.6	0
Mean Value	(μA/μm)	59.7	37.3
Standard Deviation	(μA/μm)	5.8	4.8

Table II Gate widths of Q_1 - Q_4 in Fig. 1 used in this experimental.

	SBFL-E	SBFL-D	DCFL
Q_1	D-FET 5μm	D-FET 5μm	———
Q_2	E-FET 10μm	E-FET 10μm	———
Q_3	E-FET 20μm	D-FET 5μm	D-FET 10μm
Q_4	E-FET 20μm	E-FET 20μm	E-FET 20μm

III. Circuit Fabrication

To confirm the expected properties mentioned above, the SBFL circuits were fabricated by the W-Al gate self-alignment process [3]. As a substrate, an undoped LEC semi-insulating GaAs substrate was used. Table I shows the processing conditions and the properties of obtained MESFET's. The mean values and the standard deviations shown in Table I were obtained from more than 10 samples in the area of about 10mm x 10mm. These low standard deviations in the properties of MESFET's ensured the exactness in comparison between SBFL and DCFL.

Table II shows the gate widths of Q_1-Q_4 shown in Fig. 1 used in these experiments. To measure the static transfer characteristics, the two-stage inverter chains were used. Measurements were performed on the first stage inverter. To measure propagation delay time and load drivability, 17-stage ring-oscillators with and without extra capacitance load in each stage were fabricated. Each capacitance was about 120fF with a metal-SiO_2-metal structure (18μm x 36μm).

IV. SBFL Performances

The static transfer characteristics of SBFL-E SBFL-D and DCFL are shown in Fig. 2 at the supplied voltage of 1 V. The output low level in SBFL-E is much lower than that in SBFL-D or DCFL. From these results, the following values could be obtained.

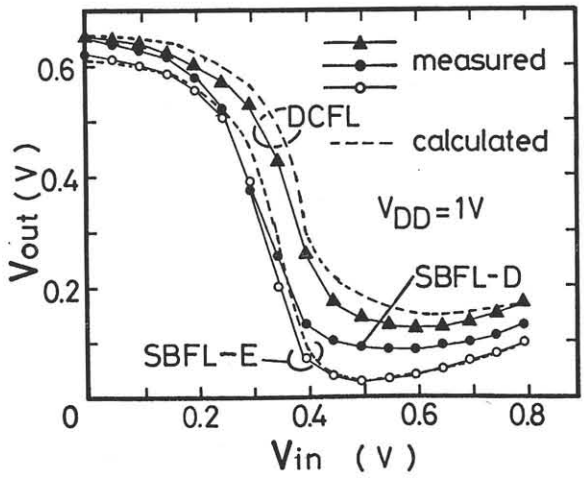

Fig. 2 The static transfer characteristics of SBFL-E, SBFL-D and DCFL at the supplied voltage of 1 V; the broken lines stand for the calculated results.

The logic swings in SBFL-E, SBFL-D and DCFL were 0.57V, 0.54V and 0.50V, respectively. The noise margins were 0.18V and 0.20V for SBFL-E, 0.14V and 0.22V for SBFL-D, and 0.15V and 0.18V for DCFL. The transfer gains were 4.0, 2.8 and 3.7 for SBFL-E, SBFL-D and DCFL, respectively. Because the high level is clamped by the next stage Schottky diodes, lower low-level of SBFL-E is attractive for steady action. In addition, the other static transfer characteristics of SBFL-E are superior to those of DCFL and SBFL-D. Therefore, later discussions are carried on about usual SBFL-E. The broken lines in Fig. 2 show the simulated results of the transfer characteristics of SBFL-E and DCFL by circuit analysis program ASTAP. The simulated values agreed relatively well with measured results.

In Fig. 3, the measured results of the unloaded propagation delay time and the current flow per gate on supplied voltage are shown ; broken lines stand for the simulated values. In the supplied voltage region of 0.8 - 1.4 V, the current of SBFL rapidly increases, in contrast to that of DCFL. In this region, the Schottky gate current rapidly increases. However, the propagation delay time of SBFL is almost constant. As the supplied voltage decreases from 0.8V, the propagation delay of SBFL rapidly increases. These characteristics are supported by the simulated results, too. Therefore, it can be concluded that the current through the Schottky gate does not contribute the decrease of propagation delay time but only increases the power dissipation in the supplied voltage region of 0.8 - 1.4V, and that the supplied voltage of less than 0.8V leads to the reduction of super-buffer motions. From Fig.3, considering both propagation delay time and power dissipation, the suitable supplied voltage for SBFL is thought to be 0.8 - 1.0 V. This voltage is almost the same as that for DCFL. Furthermore, the logic levels of SBFL are compatible to those of DCFL. Therefore, the SBFL can be successfully used along with DCFL.

Figure 4 shows the relation between the propagation delay time and the load capacitance. These data are the averages for more than 5 ring-oscillators. The supplied voltage was kept 1 V. The power dissipations with no extra capacitance are also shown in this figure. The dissipated powers are almost the same between these two kinds of circuits. The raw speed of SBFL is about 35% less than DCFL. When the load capacitance is more than about 60fF, however, the delay time of SBFL

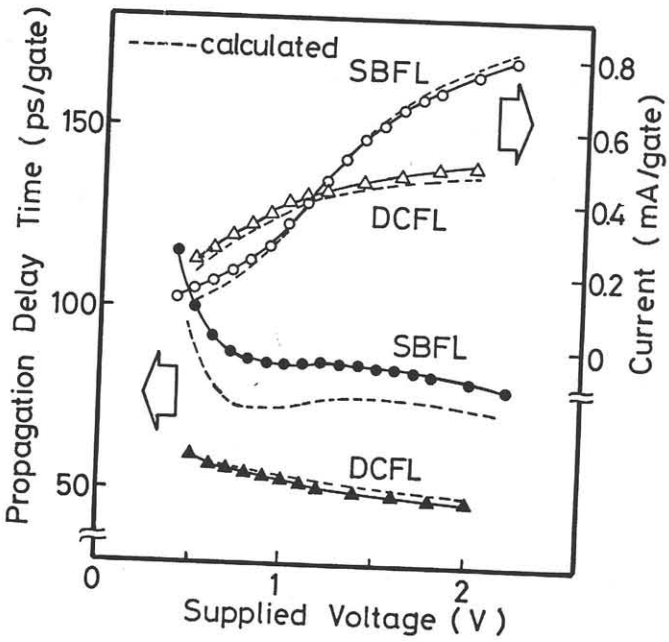

Fig. 3 The dependences of unloaded propagation delay time and current flow per gate on supplied voltages. The calculated results are also shown by the broken lines.

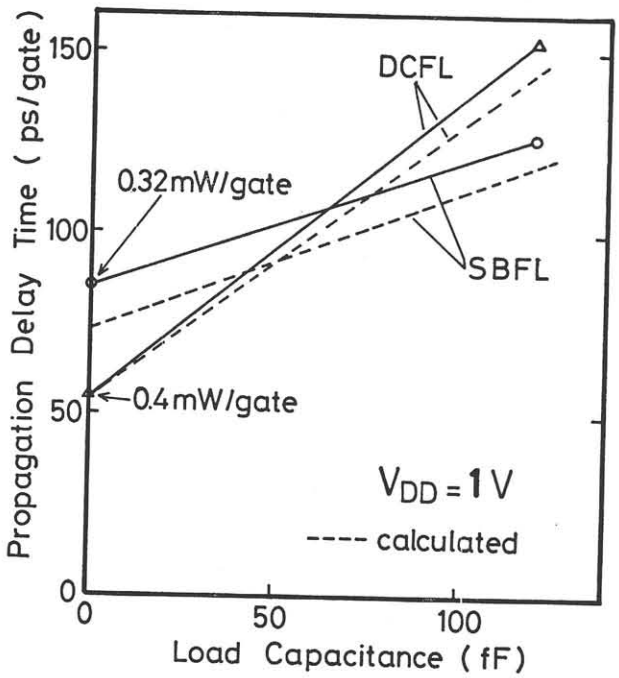

Fig. 4 The relation between propagation delay time and load capacitance at the supplied voltage of 1 V. Each point is the average for more 5 ring-oscillators. The broken lines show the calculated results.

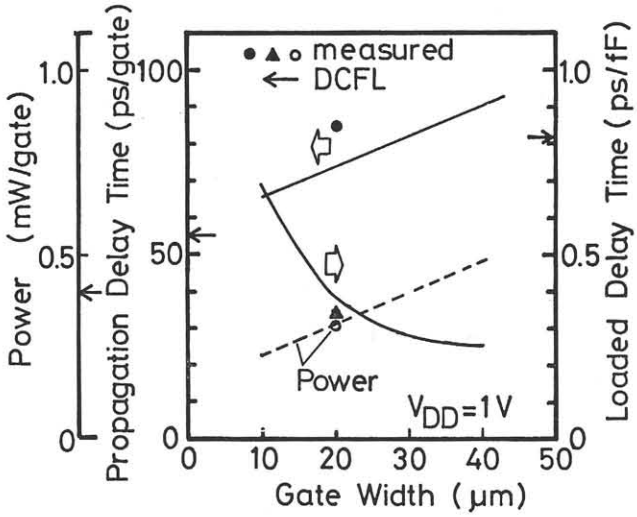

Fig. 5 The simulated results for SBFL concerning the dependences of load drivability and raw speed on the gate width of the second-stage FETs. 10μm wide E-FET and 5μm wide D-FET are used in the first-stage E/D gate.

becomes smaller than DCFL. For added load capacitance, the propagation delay time (loaded-delay time) increases by 0.34 ps/fF for SBFL and 0.82 ps/fF for DCFL. The inverse of these values can be regarded as the load drivability. So, the load drivability of SBFL is concluded to be 2.4 times larger than that of DCFL.

Figure 5 shows the simulated results concerning the dependences of load drivability and the raw speed on the gate widths of the second pull-up and pull-down FETs of SBFL. In these simulations, the gate widths of the first-stage E/D gate were assumed to be constant (W_{gE} = 10μm, W_{gD} = 5μm) and the supplied voltage was kept 1.0V. The second-stage transistors were assumed to have same gate width. In Fig. 5, the raw speed decreases and the current flow increases slightly with the increase in the gate width of the second-stage transistors. On the other hand, the loaded-delay time rapidly decreases as the gate width increases in the region of 10-20 μm. The second-stage FETs with more than 30μm gate width improve load drivability only a little. The reason is considered to be due to the too heavy load for the first-stage E/D gate. Therefore, the suitable gate widths of second-stage FETs are thought to be 20-30μm. These second-stage FETs cause the increase in the pattern size. However, the high regularity of SBFL can make the pattern size of SBFL only 30-40% larger than that of DCFL. Furthermore, the chip size of LSI made by SBFL will be only 10-20% larger than that made by DCFL because the large part of the chip area is occupied by connecting lines.

V. Summary

The super-buffer FET logic (SBFL) has been described. The SBFL circuit has lower output low-level and larger noise margins than DCFL. From the measurement of the dependence of the propagation delay time and the current flow on the supplied voltage, the suitable supplied voltage for SBFL was found to be 0.8 - 1 V. The SBFL circuit has high load drivability, which is 2.4 times larger than that of DCFL. The power dissipation is almost the same between SBFL and DCFL. It is supported by simulation that the suitable gate widths of the second pull-up and pull-down FETs were 20-30μm in case that 10μm wide E-FET and 5μm wide D-FET were used in the first-stage E/D gate.

The above results show that the SBFL circuit has large advantages for the application to GaAs LSI and VLSI. Especially, the SBFL is very suitable for large scale gate arrays, in which a high load (fan-out and connecting lines) drivability and large noise margins are strongly needed.

References

1) N.Yokoyama, T.Ohnishi, H.Onodera, T.Shinoki, A.Shibatomi, and H.Ishikawa, "A GaAs 1K static RAM using tungsten silicide gate self-aligned technology," IEEE J. Solid-State Circuits, vol. SC-18, pp.520-524, 1983.
2) K.Yamasaki, K.Asai, and K.Kurumada, "GaAs LSI-directed MESFET's with self-aligned implantation for n^+-layer technology (SAINT)," IEEE Trans. Electron Devices, vol. ED-29, pp.1772-1777, 1982.
3) H.Nakamura, Y.Sano, T.Nonaka, T.Ishida, and K.Kaminishi, "A self-aligned GaAs MESFET with W-Al gate," in GaAs IC Symp. Tech. Dig., pp.134-137, Oct. 1983.
4) Y.Nakayama, K.Suyama, H.Shimizu, N.Yokoyama, H.Ohnishi, and A.Shibatomi, "A GaAs 16 x 16 bit parallel multiplier," IEEE J. Solid-State Circuits, vol. SC-18, pp.599-603, 1983.
5) M.Hirayama, M.Ino, Y.Matsuoka, and M.Suzuki, "A GaAs 4Kb SRAM with direct coupled FET logic," in ISSCC Dig. Tech. Papers, pp.46-47, Feb. 1984.