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A GaAs HSCFL 4 GHz Divider with 60/70 ps Transition Time

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4 GHz GaAs frequency divider IC's with less than 70 ps output wave fall/rise time (20-80%) have been developed using a new logic circuit configuration, High logic voltage swing Source Coupled FET Logic (HSCFL). Along with high speed performance, high fabrication yields are obtained (for example, 75 % for 1/2 divider).

These results are due to the special advantages HSCFL presents and the use of submicron gate SAINT FET's fabricated with electron beam lithography. The features of HSCFL are high f_T voltage range operation, a large noise margin and a wide permissible range for FET threshold voltage shift.

(1) Introduction

To develop the GaAs LSI or VLSI, the use of enhancement type FET's (EFET's) are preferable for low power dissipation and simplicity of circuit configuration. Several attempts [1),2)] at developing LSI/VLSI's have been carried out using E/D DCFL to confirm feasibility. However, because EFET's have a low cut-off frequency, f_T, ultra high speed performance for GaAs IC's cannot be expected. For high speed requirements, large pinch-off voltage depletion type FET's are preferable.

The authors realized high speed frequency dividers using High logic voltage swing Source Coupled FET Logic (HSCFL) which adopted very low threshold voltage FET's ($V_{TH} \simeq -1.0$ v) and gave them noticeably high logic voltage swing ($\simeq 2.8$ v) operation. HSCFL is an improvement on SCFL, which we first proposed, [3),4)] for high speed performance and a large noise margin. Both HSCFL and SCFL have the advantage of a wide permissible range from the designed value for the threshold voltage shift. Therefore, HSCFL promises not only high speed but also high production yield.

This paper describes the HSCFL design concept, the 1/2 and 1/8 frequency divider design using HSCFL, the fabrication process, and measurement results.

(2) HSCFL Design Concept

The fundamental HSCFL circuit configuration is the same as SCFL, as shown in Fig.1. For high speed operation, it is commonly known that FET's which have high transconductances (g_m) and small capacitances should be fabricated by reducing gate lengths (lg) and omitting parasitic resistances and capacitances. In addition, optimization of the FET operating condition is significantly effective for increasing the circuit maximum operating frequency. The logic swing design is a key in this optimization. Bias voltage dependences of f_T ($g_m/2\pi C_{gs}$, C_{gs}: gate-to-source capacitance) for two different V_{TH} GaAs MESFET's are shown in Fig.2. In this figure, g_m is the measured value and C_{gs} is the calculated value. Except for the impurity dose, these two FET types were fabricated by the same process. The FET with lower V_{th} (No.1) has a much higher maximum f_T than that with higher

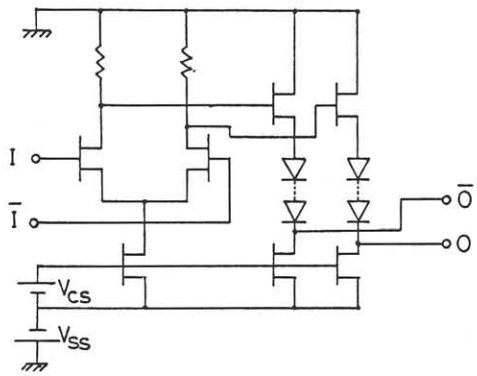


Fig.1 HSCFL circuit configuration

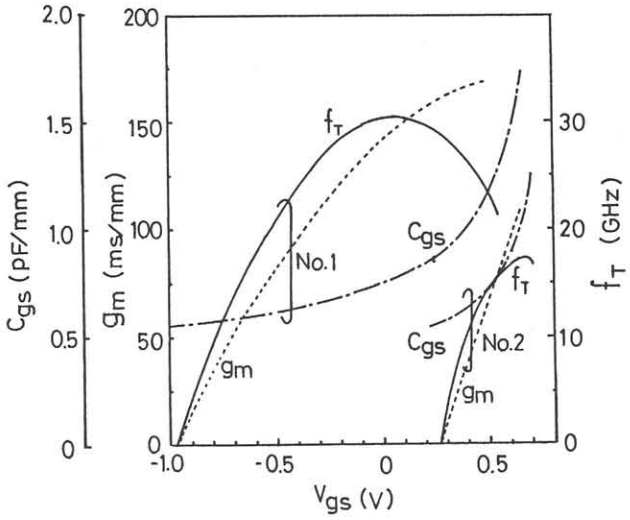


Fig.2 V_{gs} dependence of f_T, g_m, and C_{gs} as a parameter of V_{TH}. V_{TH}'s for No.1 and No.2 FET are -1.0 and 0.25 V, respectively. l_g is 0.7 um.

V_{TH} (No.2). However, a maximum f_T is not a direct figure of merit in a logic circuit, since FET's operate in a wide V_{gs} range from off-voltage to on-voltage, V_{on}. We found from circuit simulation results that average f_T ($\equiv\overline{f_T}$) defined by following equation was a suitable figure of merit for circuit speed.

$$\overline{f_T} \equiv \frac{1}{V_{sw}} \int_{V_{TH}}^{V_{on}} f_T \, dV_{gs} \quad \text{-----(1)}$$

, where V_{sw} is expressed as

$$V_{sw} = V_{on} - V_{TH} \quad \text{-----(2)}$$

The calculated results of $\overline{f_T}$ for No.1 and No.2 FET are shown in Fig.3. It is found that $\overline{f_T}$ has a different optimum V_{sw} when it has a different V_{th}. It should be noted that $\overline{f_T}$ for No.1 is lower than that of No.2 at small V_{sw} range. This means that even if FET V_{th} was low and had very high maximum f_T, high speed performance could not be obtained without a large V_{sw}.

The V_{sw} is related to a voltage logic swing V_{LS} as

$$V_{LS} = 2V_{nm} + V_{sw} \quad \text{-----(3)}$$

, where V_{nm} is noise margin. The larger noise margin permits a higher fabrication yield. Thus, for high speed and high yield IC's, use lower V_{th} FET's with a large logic swing.

However, since HSCFL requires a much higher voltage source ($\gtrsim$8V) than usual SCFL ($\simeq$5V) or other logic schemes due to the large logic swing, it is difficult to produce a low power circuit.

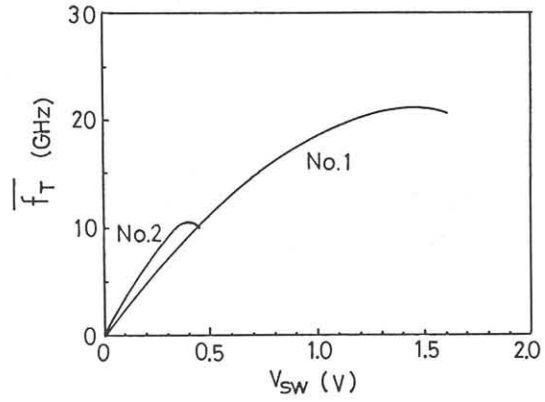


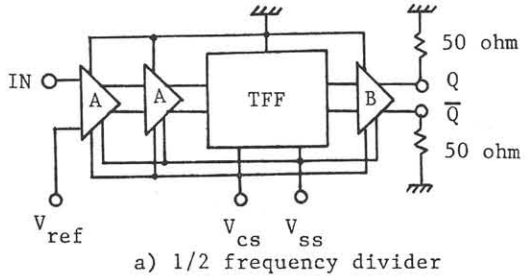
Fig.3 Average f_T switching voltage dependence

Therefore, it is better suited for SSI/MSI desired special high speed performance rather than LSI/VLSI's.

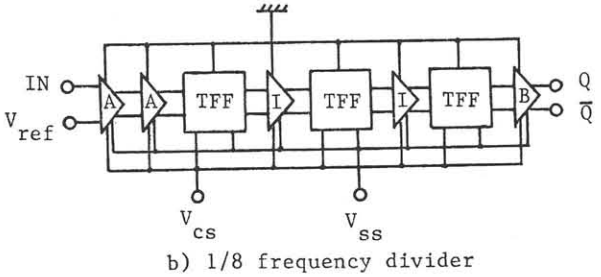
(3) Frequency divider design

To verify the HSCFL features, 1/2 and 1/8 frequency dividers were designed and fabricated. Configurations of the dividers, consisting of two stage input amplifiers, T-type flip/flop's, inverters and output buffers are shown in Fig.4. T-F/F's were constructed by two level series gating master-slave F/F that were commonly used in SCFL[4),5)] or ECL circuits.

The designed value for FET V_{TH} was -1.0 V. V_{sw} were determined from Fig.3 to 1.4 V, and V_{nm} was to 0.7 V. This means that the internal logic



a) 1/2 frequency divider



b) 1/8 frequency divider

Fig.4 Divider constructions. A, B and I are input amplifier, output buffer and inverter, respectively.

voltage swing is as high as 2.8 V.

The input differential amplifiers are added in front of the T-F/F in order to convert from an ECL logic swing to a 2.8 V HSCFL logic swing. If logic circuit systems are constructed only using HSCFL, these amplifiers are not necessary except to input interface from other logic levels.

An inverter was inserted between T-F/F's to reduce the fan-out effect in the 1/8 divider. An open-drain inverter was used as an output buffer for the 1/2 divider. The buffer intentionally reduces the logic voltage swing from 2.8 V to 0.7 V for a 50 ohm load. This reduction permits a very rapid output wave transion because of the buffers small input capacitance. The buffer for the 1/8 divider was also an inverter with internal 100 ohm resistors.

The buffers in the 1/2 and 1/8 dividers have Q and $\overline{Q}$ complemental outputs. For investigating the shield effects of signal waves, different pattern layouts of output lines to pads were carried out. Q output node at the buffer was connected to the output pad with a coplanar 50 ohm line while $\overline{Q}$ output node was with a high impedance line of about 200-300 ohm. The significant output waveform differences between the two layouts were measured. The results are described in Section (5).

(4) Fabrication process

The IC's were fabricated by the EB-SAINT [6] process to realize submicron gate length (0.8 μm) and to reduce gate parasitic capacitances which significantly decrease the circuit maximum operating frequency, especially for gate-to-drain parasitic MOS capacitance.

We fabricated two wafers which had V_{TH}'s of -0.8 and -1.0V and g_m's of 130 and 150 mS/mm at 0V V_{gs}, respectively. Both wafers, processed from 0.1-0.3 wt-ppm chromium doped LEC grown semi-insulated 2 inch size substrates, had the same V_{TH} standard deviation of 130 mV. A 500 ohm sheet resistance n^+ layer for resistive loads was used because of good reproducibility and a small standard deviation of 3.1-3.9 %.

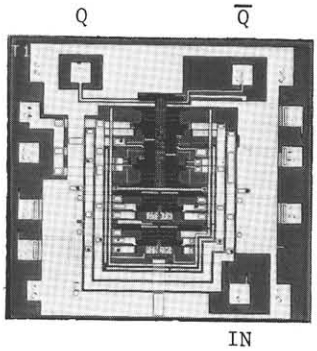


Fig.5 Microphotograph of the 1/2 divider.

The microphotograph of Fig.5 shows a fabricated 1/2 divider. Chip size is 1.4×1.5 mm. The chip size of the 1/8 divider is 1.5×2.5 mm.

(5) Measurement result

Measurements were mainly carried out with an on-wafer high frequency probe-card developed in our laboratory. This card has 1.2 mm diameter coaxial probes for signal leads and is able to measure from dc to 7.5 GHz. There was no significant difference between in-package and on-wafer measurements. All of the following results are obtained using the on-wafer test system.

Fig.6 shows a maximum toggling operation at 4.03 GHz for a 1/2 divider. We also measured a very small fall/rise time of 60/70 ps (20-80%) using the same chip at lower frequency operation

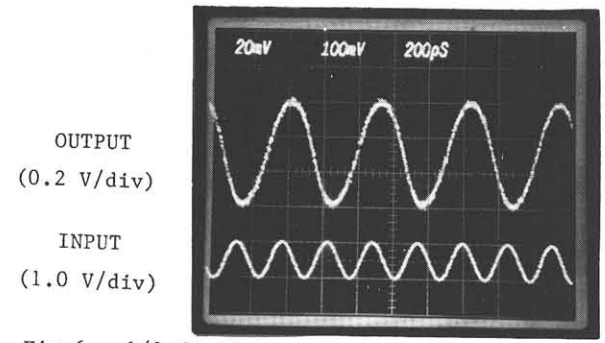


Fig.6 1/2 divider maximum toggling frequency operation at 4.03 GHz. Output load is 50 ohm.

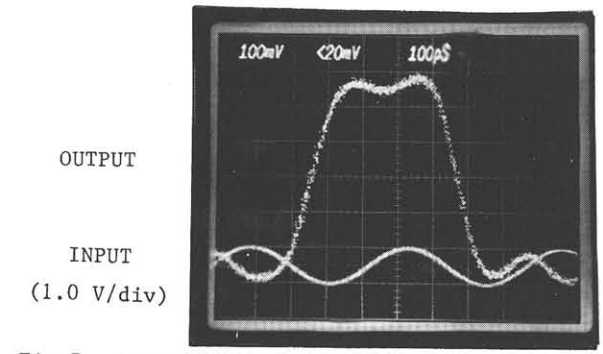


Fig.7 Output-wave t_f/t_r measurement result for 1/2 divider. Input frequency is 2.3 GHz. Output load is 50 ohm.

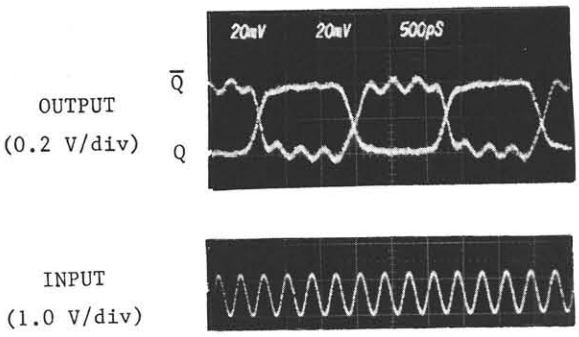


Fig.8 Q and $\overline{Q}$ output waveforms of the 1/8 divider. output load is 50 ohm.

(2.3 GHz) as shown in Fig.7. The value of the fall/rise time is one of the best results to date. Typical supplied voltage and power dissipation were -8 V and 1.1 W including input amplifiers. The power dissipated in the amplifier is 0.6 W.

Q and $\overline{Q}$ output waveforms of the 1/8 divider at 3.1 GHz input frequency are shown in Fig.8. $\overline{Q}$ output waveform includes input wave leakage. This phenomenon took place above 2.7 GHz. On the other hand, Q output, whose lead line to the pad is designed with a 50 ohm coplanar line, always has a pure waveform. It is clear that the pattern layout affects signal waveform seriously above about 3 GHz operation in GaAs IC's due to the use of a semi-insulated substrate. The maximum operating frequency for a 1/8 divider, which has lower power gates than a 1/2 divider, was 3.4 GHz. 1/8 divider power was 0.7 W including input amplifiers.

The toggle frequency histogram of 1/2 divider chips on the two wafers mentioned above is shown in Fig.9. The chip yield is as high as 75 %. Among successfully fabricated chips, 89 % operated above 3.5 GHz. For the 1/8 divider, all of the successful chips operated above 3 GHz and its yields were 60 %. Failed chips almost always had a photolithography pattern defect.

(6) Conclusion

The feasibility of high-yield GaAs HSCFL G-bits digital SSI/MSI's has been confirmed through the development of 1/2 and 1/8 frequency dividers.

The output wave fall/rise time, the maximum toggling frequency and the processed two wafers chip yield for the 1/2 divider were 60/70 ps (20-80%), 4.03 GHz and 75%, respectively.

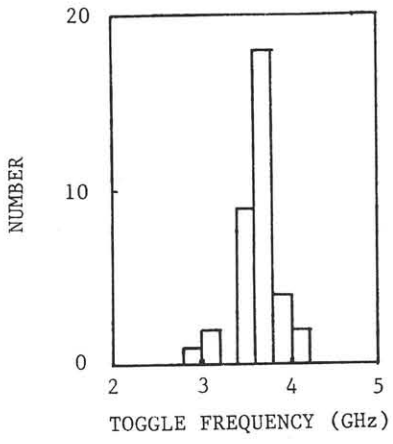


Fig.9 Toggle frequency histogram of chips fabricated on two wafers for 1/2 divider.

The shield effect of the signal wave was also analysed, and a pure output waveform without input wave leakage was obtained for the 1/8 divider.

These excellent results are due to the high logic voltage swing of HSCFL and high f_T SAINT MESFET's with an EB writing submicron gate.

Acknowledgement

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