

Photo-CVD Dielectric Films on InP

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The characteristics of Si_3N_4 and SiO_2 on InP by photo-CVD method are investigated on their physical, chemical and electrical properties in view of application for MISFETs. Especially their deposition temperature dependence and the effects of post-annealing are studied.

The double gate depletion mode InP MISFETs are fabricated using photo-CVD Si_3N_4 . The good RF output characteristics are obtained showing that photo-CVD Si_3N_4 is very promising as the gate insulator of InP MISFETs.

1. INTRODUCTION

InP is an attractive material for high frequency power FETs because of its high peak velocity, low ionization coefficients and good thermal conductivity.⁽¹⁾ The achievement of stable insulator/InP interface with low surface state density is the key technique to realize the high performance InP MISFETs. Recently, several reports have been published on InP MIS interface with low surface state density, as example, anodic Al_2O_3 /native oxide double-layer⁽²⁾ or CVD SiO_2 .⁽³⁾ However, many problems are left to apply those dielectrics for FETs process.

InP decomposes easily at relatively low temperature because of vaporization of phosphorous elements, so it is necessary to control the process temperature less than 300°C.⁽⁴⁾ The photochemical vapor deposition(photo-CVD) method is a very promising technique from a viewpoint of low temperature deposition of dielectrics on InP. However, there are few publications on characteristics of the interface between InP and dielectrics deposited by photo-CVD method.

In this report the characteristics of Si_3N_4 and SiO_2 deposited on InP by the photo-CVD method are discussed on their physical, chemical and electrical properties in view of application for MISFETs' gate insulator. Especially the effects of deposition temperature and post-annealing are examined in detail. Characteristics of the InP MISFETs using photo-CVD Si_3N_4 as the gate insulator

are also discussed.

2. EVALUATION OF MIS INTERFACES

Experimental

The substrates were non-dope n-type InP with carrier concentrations of about $6 \times 10^{15} \text{cm}^{-3}$ and with $\langle 100 \rangle$ orientation. After surface cleaning, Si_3N_4 or SiO_2 was deposited (about 1000 Å thickness) on the substrates at several temperature, using ultraviolet light with reagent gases such as $\text{SiH}_4 + \text{NH}_3$ or $\text{SiH}_4 + \text{N}_2\text{O}$ respectively, by mercury sensitization method. Refractive indices and thickness of the films were measured by ellipsometry, and stoichiometry was characterized by infrared spectroscopy. Characteristics such as C-V curves, $I - \sqrt{V}$ curves and breakdown field strength of the films were measured using MIS diodes of 400 μm diameter (Au/ Si_3N_4 or SiO_2 /n-InP/ AuGe/ Ni/ Au). Post-annealing was carried out in N_2 or H_2 atmosphere at 400°C or 600°C.

Results and discussion

Dependence of etch rate and refractive indices of Si_3N_4 and SiO_2 upon deposition temperature are shown in Fig.1. Etch rate of both films decrease with increase of deposition temperature, while refractive indices of both films increase. These may be due to decrease of porosity and strain in the films. Low refractive indices of Si_3N_4 deposited at low temperature are probably due to high contents of hydrogen atoms. This is confirmed

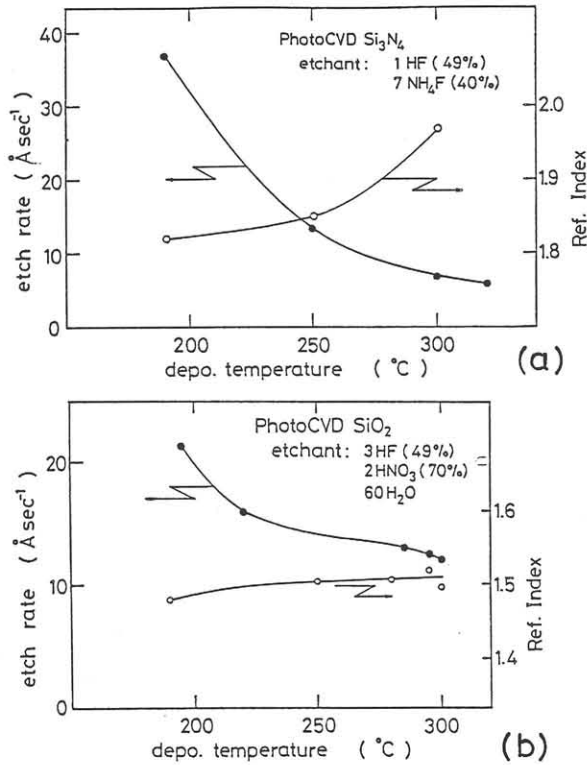


Fig.1. Deposition temperature dependence of etch rate and refractive indices of (a) Si_3N_4 , and (b) SiO_2 .

by measurements of infrared spectra.⁽⁵⁾ Refractive indices of SiO_2 are a little higher than those of well-known pyrolytic SiO_2 . This discrepancy of refractive indices may be due to silicon enrichment and be improved by optimization of the deposition condition.

The C-V curves of Si_3N_4 and SiO_2 deposited at 300°C and annealed at 400°C in N_2 atmosphere for 20 mins are shown in Fig.2. Hysteresis of Si_3N_4 measured at 1MHz is about 1V, and frequency dispersion at accumulation side is very little. Hysteresis of SiO_2 are slightly larger than that of Si_3N_4 , and the C-V curves at lower frequency than 1MHz could not be measured due to its unstability. Hysteresis was not improved by post-annealing, while surface state density and frequency dispersion of dielectric constants were significantly improved as mentioned below.

Distributions of surface state density of Si_3N_4 and SiO_2 deposited at 300°C is shown in Fig.3, which are calculated by Terman method. Minimum values of surface state density become lower by post-annealing and by increasing of deposition temperature. Remarkable reduction of surface state density by post-annealing is observed

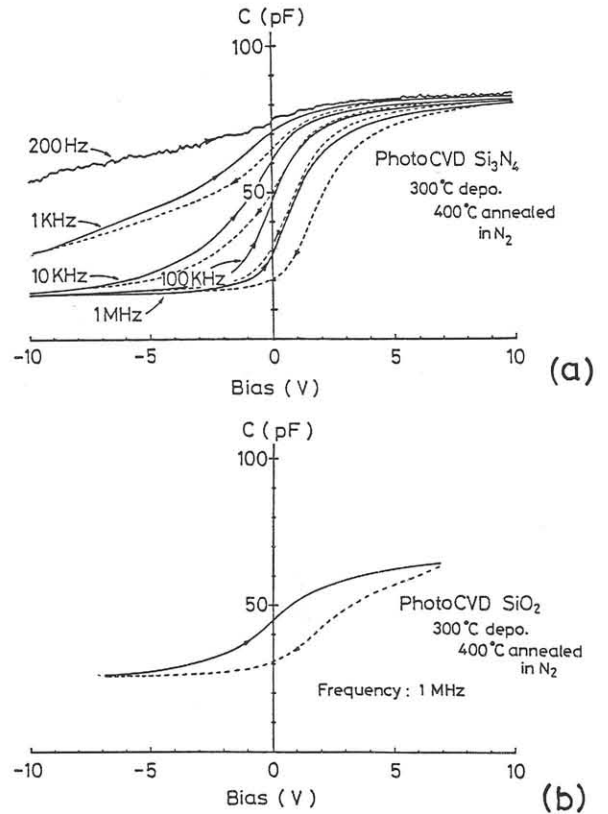


Fig.2. The C-V curves of (a) Si_3N_4 , and (b) SiO_2 .

with Si_3N_4 . The minimum surface state density of $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ with Si_3N_4 annealed at 400°C is thought to be less enough for the application to MISFETs.

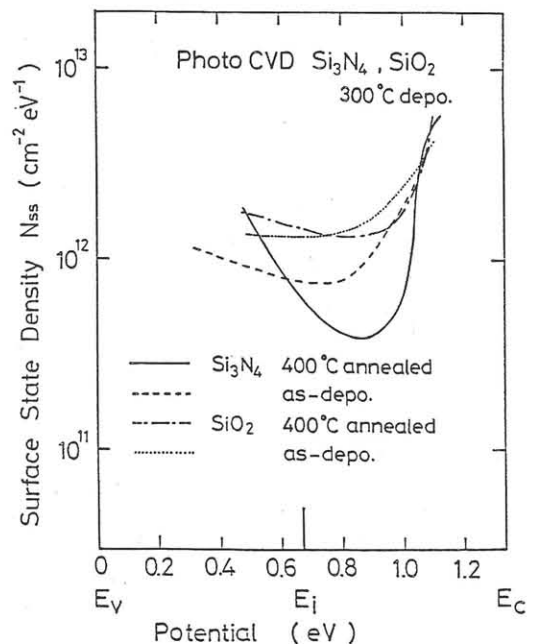


Fig.3. Distribution of the surface state density of Si_3N_4 and SiO_2 .

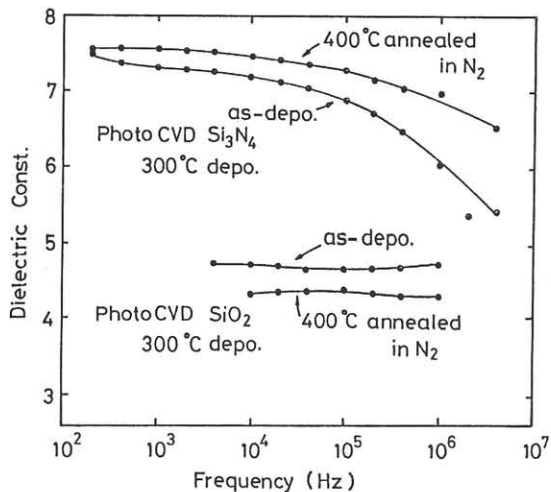


Fig. 4. Frequency dispersion of the dielectric constants of Si_3N_4 and SiO_2 .

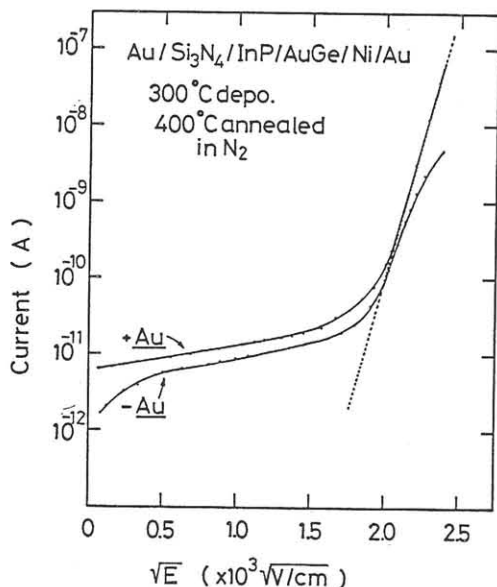


Fig. 5. Poole-Frenkel plots of I-V characteristics of Si_3N_4 .

Frequency dispersion of dielectric constants of Si_3N_4 and SiO_2 calculated with C-V curves are shown in Fig. 4. Dielectric constants of Si_3N_4 increase by annealing at 400°C due to removal of hydrogen atoms. In contrast those of SiO_2 decrease by annealing.

The Poole-Frenkel plots of I-V characteristics of Si_3N_4 are shown in Fig. 5. These plots show well-known two stages of conduction. The dotted line shows conduction due to Poole-Frenkel effect. The dielectric constant calculated with this slope is 3.9.

Breakdown field strength of the both films was measured with curve tracer. In this experiment it is defined that the breakdown field strength is

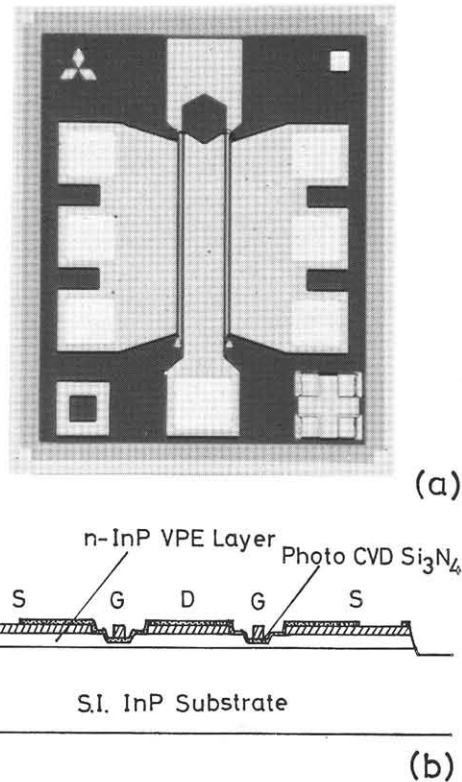


Fig. 6. (a) The geometry and (b) the schematic cross sectional view of the MISFETs.

the electric field at which current of $10\ \mu\text{A}$ flows in a MIS diode. Breakdown field strength of Si_3N_4 and SiO_2 are about $9 \times 10^6\ \text{V/cm}$ which are higher than the ever reported values of Al_2O_3 /native oxide system and are comparable to those of conventional CVD SiO_2 .

3. InP MISFETs

The double gate depletion mode InP MISFETs were fabricated using photo-CVD Si_3N_4 as the gate insulator. Fig. 6 shows the geometry and the schematic cross sectional view of the MISFETs. The source-drain spacing is $5\ \mu\text{m}$, gate length is $1.5\ \mu\text{m}$ and useful gate width is $360\ \mu\text{m}$.

The n-InP epitaxial layers were grown on Fe-doped semi-insulating substrates by chloride VPE technique. Their thickness was about $0.5\ \mu\text{m}$ and the carrier concentrations were about $2 \times 10^{17}\ \text{cm}^{-3}$. AuGe/Ni ohmic contacts for source and drain regions were fabricated by evaporation and the ordinary lift-off technique. After mesa definition, the channel was recessed using $\text{H}_3\text{PO}_4 + \text{HCl}$ (9:1) etchant. The Si_3N_4 gate insulator was deposited at 300°C by the above mentioned photo-CVD technique and then annealed at 400°C for 20 mins in N_2 atmosphere. The thickness of the Si_3N_4 film was

about 1000 Å. The Ni/Au gate, 5000 Å thick, was formed by evaporation and finally the windows were opened in the source and drain region for bonding areas.

Fig.7 shows the typical I-V characteristics. The transconductance shown in this figure is about 20 mmS/mm, while at 80 μ sec pulsed gate bias mode it becomes 40 mmS/mm. This means that the higher surface potential excursion occurs at higher frequency gate bias, as the case observed with conventional CVD SiO₂ gate insulator.⁽¹⁾ The loop in the I-V curve may be mainly due to the hysteresis of the gate insulator.

The output power at 8 GHz with 14.5V drain bias is plotted in Fig.8 as a function of input power. The linear gain is about 9 dB and 1 dB

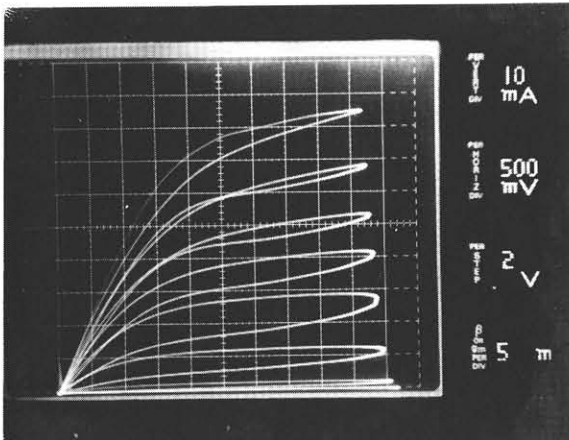


Fig.7. Drain current-voltage characteristics for the InP MISFET.

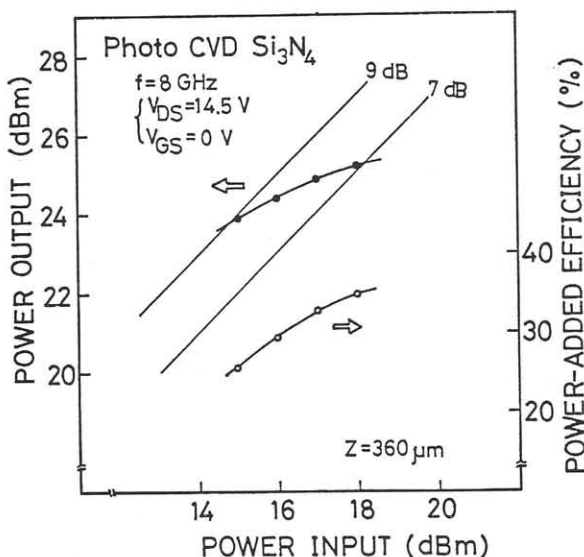


Fig.8. Power input-to-output responses at 8 GHz.

compression is at 310 mW (0.86 W/mm) output power with 33 % power added efficiency. The measured highest output power of 370 mW (1 W/mm) is obtained at 16.2 V drain bias with 32 % power added efficiency. The long term drifts of drain currents and RF output power are not observed when RF characteristics are measured. Considering that the parameters of the fabricated FETs are not optimized for power devices, these RF output characteristics are excellent showing the good quality of the photo-CVD Si₃N₄ as the gate insulator for InP MISFETs.

4. CONCLUSION

The quality of photo-CVD Si₃N₄ and SiO₂ on InP are found to be improved with increase of deposition temperature from the results of etch rate, refractive indices and infrared spectra measurements.

The characteristics of MIS interfaces tend to be improved by post-annealing. The minimum surface state density of $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ is obtained with photo-CVD Si₃N₄ annealed at 400°C.

InP MISFETs using photo-CVD Si₃N₄ as the gate insulator have the excellent RF output characteristics at 8 GHz of 9 dB linear gain and 310 mW (0.86 W/mm) output power with 33 % power added efficiency at 1 dB gain compression point.

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